杰力科技股份有限公司
Excelliance MOS Corporation

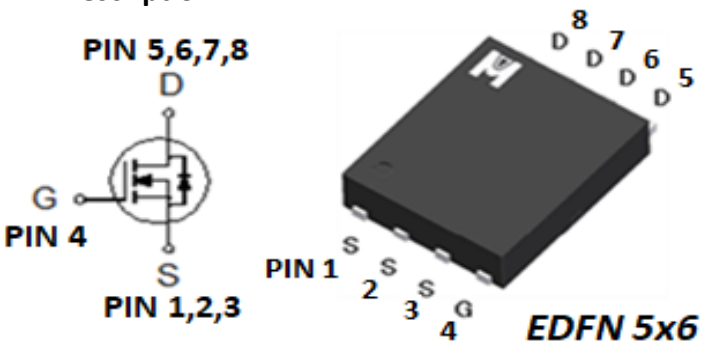
EMP85N10H

Single N-Channel Logic Level Enhancement Mode Field Effect Transistor

▪Product Summary:

	N-CH
BVDSS	100V
$R_{DSON\ (MAX.)}$@V_{GS}=10V	7.5mΩ
$R_{DSON\ (MAX.)}$@V_{GS}=4.5V	10.0mΩ
I_D @T_C=25°C	107.0A
I_D @T_A=25°C	14.0A

▪ Pin Description:



Single N Channel MOSFET
UIS, Rg 100% Tested
Pb-Free Lead Plating & Halogen Free

GP
GREEN PRODUCT

▪ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_C = 25 °C	I_D	107	A
	T_C = 100 °C		68	
Continuous Drain Current	T_A = 25 °C	I_D	14	
	T_A = 70 °C		11	
Pulsed Drain Current[1]		I_{DM}	169	
Avalanche Current		I_{AS}	30	
Avalanche Energy	L = 0.1mH	EAS	45.0	mJ
Repetitive Avalanche Energy[2]	L = 0.05mH	EAR	22.5	
Power Dissipation	T_C = 25 °C	P_D	138.9	W
	T_C = 100 °C		55.6	
Power Dissipation	T_A = 25 °C	P_D	2.5	W
	T_A = 70 °C		1.6	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

▪ 100% UIS testing in condition of VD=50V, L=0.1mH, VG=10V, IL=18A, Rated VDS=100V N-CH

▪THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		0.9	°C/W
Junction-to-Ambient[3]	$R_{\theta JA}$		50	

[1]Pulse width limited by maximum junction temperature.
[2]Duty cycle < 1%
[3]50°C / W when mounted on a 1 in^2 pad of 2 oz copper.
[4]Guarantee by Engineering test

▪ **ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)**

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage[4]	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250uA	100			V
Gate Threshold Voltage[4]	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250uA	1.5	2	2.5	
Gate-Body Leakage[4]	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current[4]	I_{DSS}	V_{DS} =80V, V_{GS} = 0V			1	uA
		V_{DS} =70V, V_{GS} =0V, T_J = 125°C			25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 5V, V_{GS} = 10V	107			A
Drain-Source On-State Resistance[1,4]	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 24A		6.2	7.5	mΩ
		V_{GS} = 4.5V, I_D = 20A		7.6	10	
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 24A		70		S
DYNAMIC						
Input Capacitance[5]	C_{iss}	V_{GS} = 0V, V_{DS} = 50V, f = 1MHz		2852		pF
Output Capacitance[5]	C_{oss}			500		
Reverse Transfer Capacitance[5]	C_{rss}			30		
Gate Resistance[4,5]	R_g	f = 1MHz		1.0		Ω
Total Gate Charge[1,2,5]	Q_g(V_{GS}=10V)	V_{DS} = 50V, V_{GS} = 10V, I_D = 24A		40.5		nC
	Q_g(V_{GS}=4.5V)			21.2		
Gate-Source Charge[1,2,5]	Q_{gs}			7.7		
Gate-Drain Charge[1,2,5]	Q_{gd}			7.6		
Turn-On Delay Time[1,2,5]	$t_{d(on)}$	V_{DS} = 50V, V_{GS} = 10V, I_D = 5A , Rg = 6Ω		12.0		nS
Rise Time[1,2,5]	t_r			11.4		
Turn-Off Delay Time[1,2,5]	$t_{d(off)}$			44.3		
Fall Time[1,2,5]	t_f			37.8		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				107	A
Pulsed Current[3]	I_{SM}				169	
Forward Voltage[1,4]	V_{SD}	I_F = 24A, V_{GS} = 0V			1.2	V
Reverse Recovery Time[5]	t_{rr}	I_F = 40A, dI_F/dt = 100A / uS		49.5		nS
Peak Reverse Recovery Current[5]	$I_{RM(REC)}$			2.11		A
Reverse Recovery Charge[5]	Q_{rr}			57.9		nC

[1]Pulse test : Pulse Width ≦ 300 usec, Duty Cycle ≦ 2%.

[2]Independent of operating temperature.

[3]Pulse width limited by maximum junction temperature.

[4]Guarantee by FT test Item

[5]Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.

▪TYPICAL CHARACTERISTICS

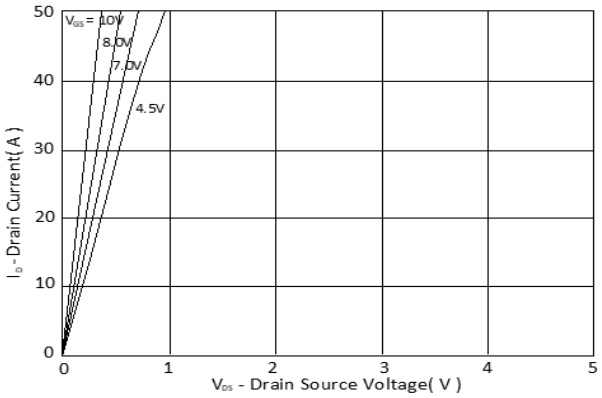


Fig.1 Typical Output Characteristics

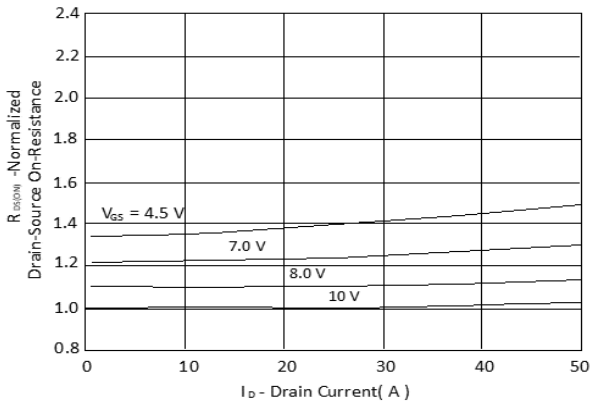


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

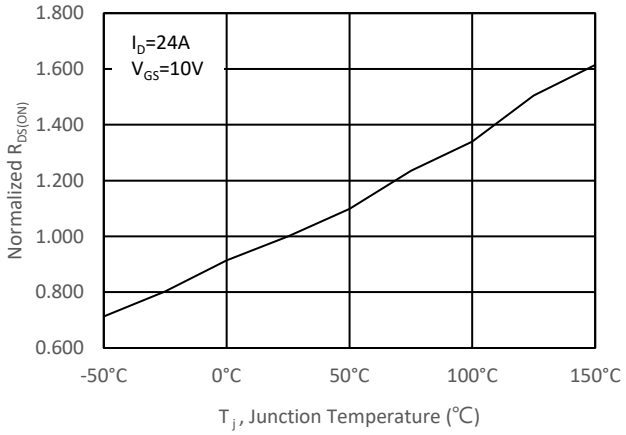


Fig.3 Normalized On-Resistance v.s. Junction Temperature

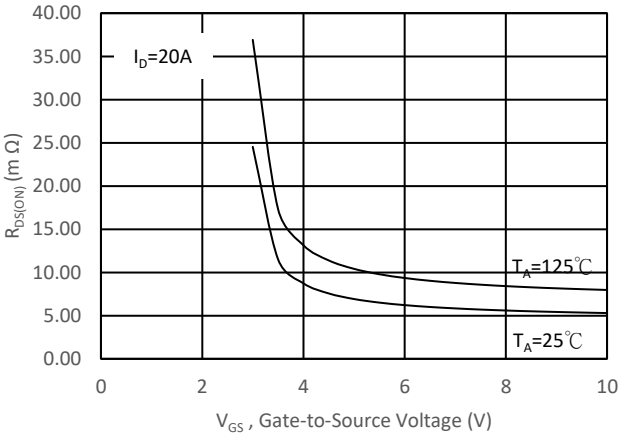


Fig.4 On-Resistance v.s. Gate Voltage

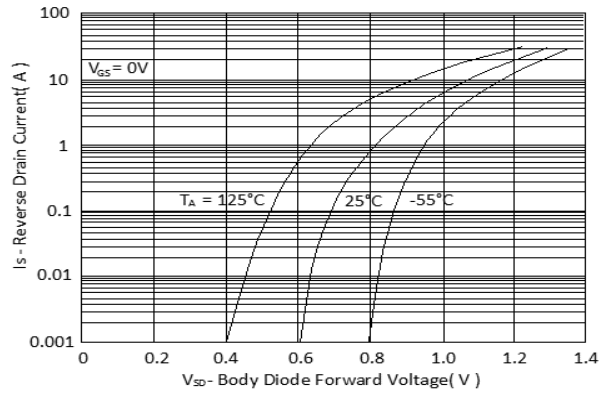


Fig.5 Forward Characteristic of Reverse Diode

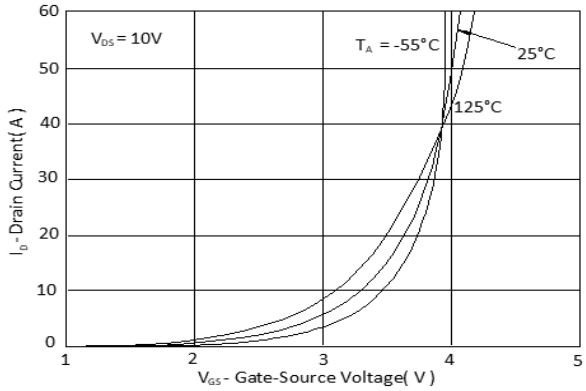


Fig.6 Transfer Characteristics

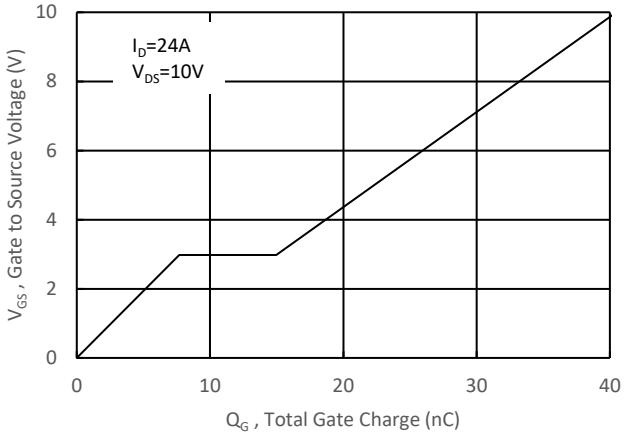


Fig.7 Gate Charge Characteristics

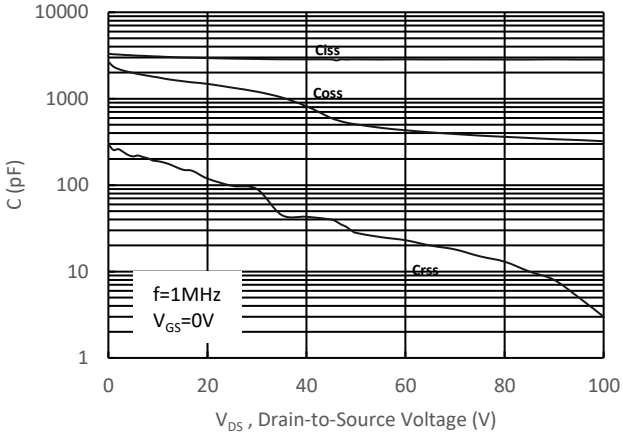


Fig.8 Typical Capacitance Characteristics

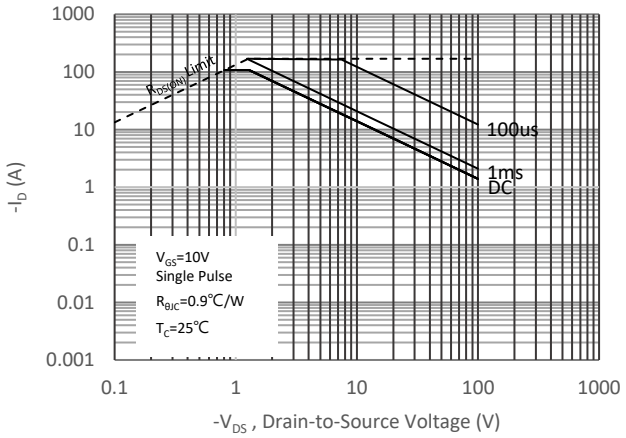


Fig 9. Maximum Safe Operating Area

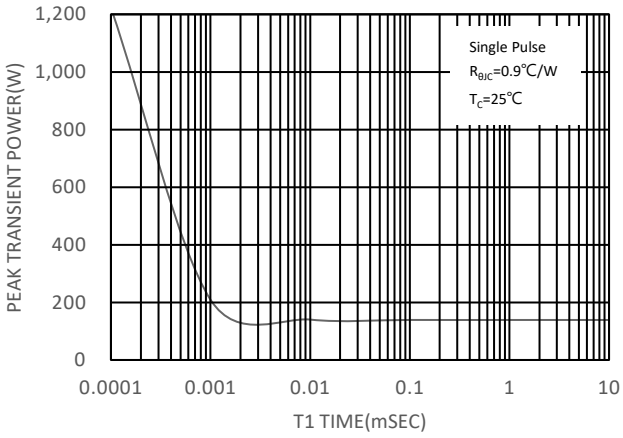


Fig 10. Single Pulse Maximum Power Dissipation

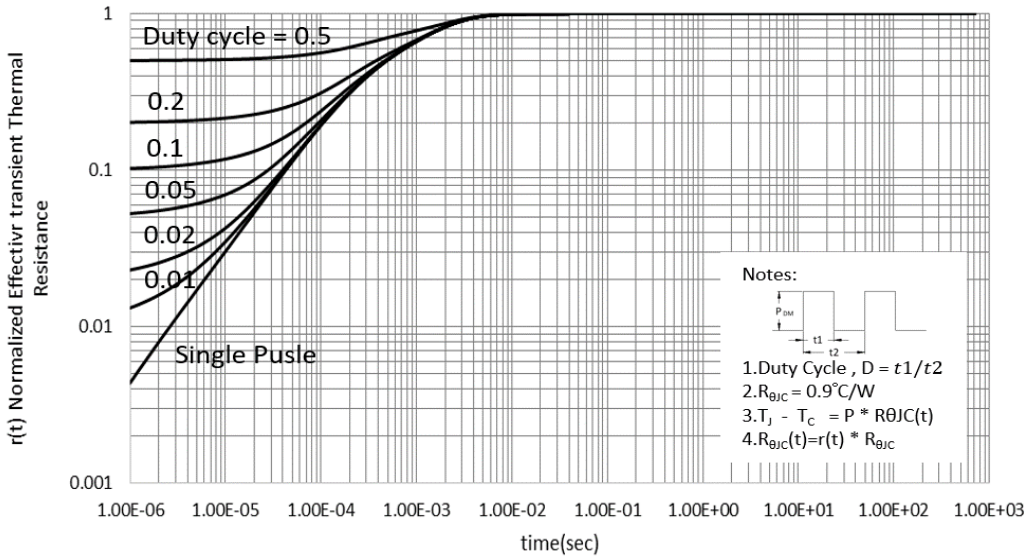


Fig 11. Effective Transient Thermal Impedance

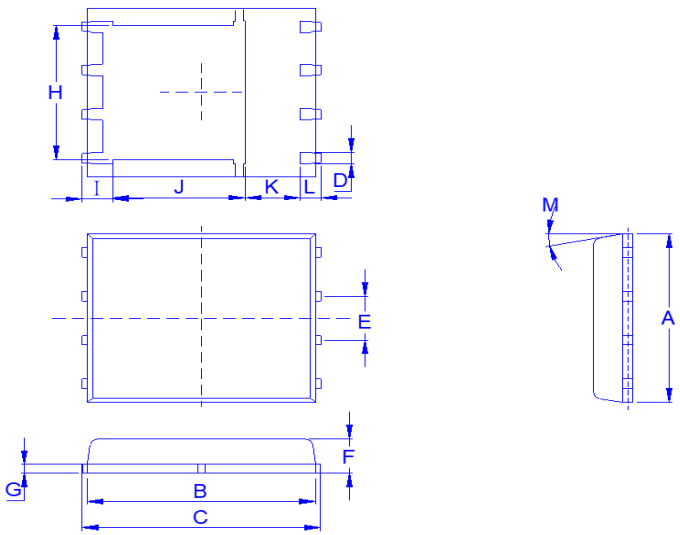
Ordering & Marking Information:

Device Name: EMP85N10H for EDFN 5x6

P85N10: Device Name

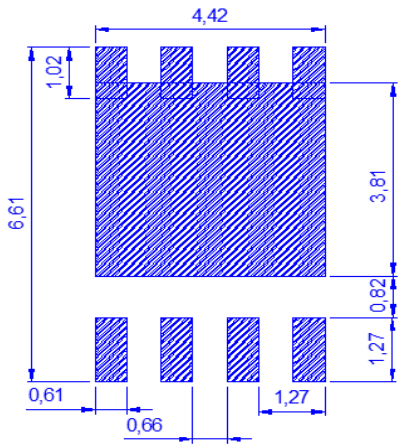
ABCDEFG: Date Code
A: Assembly House
B: Year(A:2008 B:2009 C:2010….)
C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)
DEFG: Serial No.

Outline Drawing

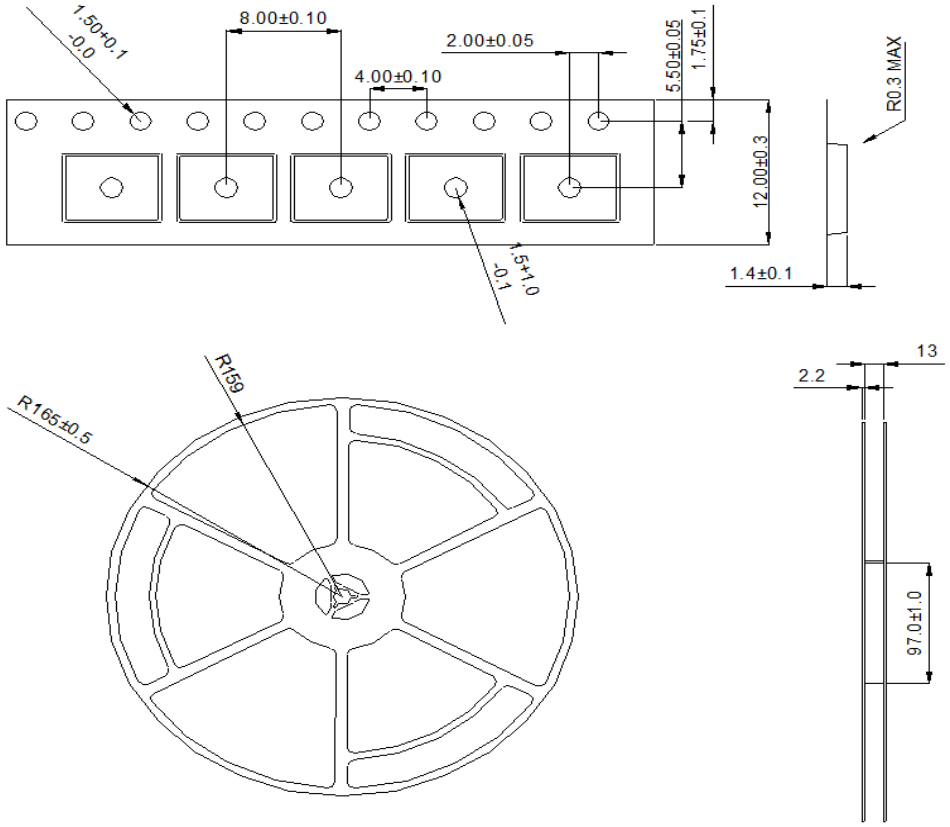


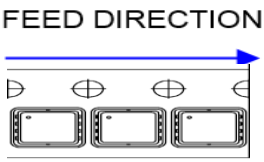
Dimension	A	B	C	D	E	F	G	H	I	J	K	L	M
Min.	4.8	5.55	5.9	0.3	1.17	0.85	0.15	3.61	0.38	3.18	1	0.38	0°
Typ.	4.9	5.7	6	0.4	1.27	0.95	0.2	3.87	0.4	3.44	1.2	0.4	
Max.	5.4	5.85	6.15	0.51	1.37	1.17	0.34	4.31	0.71	3.78	1.39	0.71	12°

Footprint



◆ **Tape&Reel Information:2500pcs/Reel (Dimension in millimeter)**



產品別	EDFN 5x6
Reel尺寸	13"
編帶方式	
前空格	25
後空格	50
裝箱數	
滿捲數量	2.5K
捲/內盒比	01:01
內盒滿箱數	2.5K
內/外箱比	10:01
外箱滿箱數	25K

★Datasheet Latest version specification :

	Revision History	Prepared	Approved	Date
A.0	Initial Datasheet	Jannie	Andy	2017/6/20
A.1	Add revised elements according to the requirements of the new version	Johnson	Sam	2020/6/18