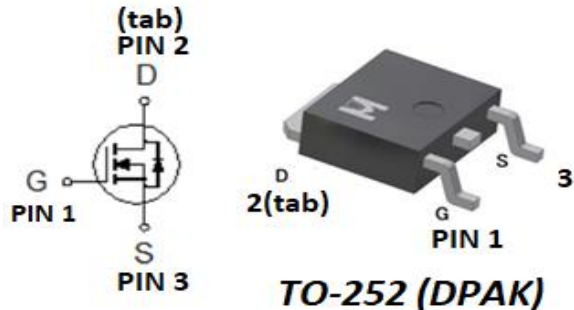


Single N-Channel Logic Level Enhancement Mode Field Effect Transistor

•Product Summary:

	N-CH
BVDSS	30 V
$R_{DSON (MAX.)@V_{GS}=10V}$	3.5 mΩ
$R_{DSON (MAX.)@V_{GS}=4.5V}$	5.0 mΩ
$I_D @T_C=25^{\circ}C$	103 A
$I_D @T_A=25^{\circ}C$	16 A

• Pin Description:



Single N Channel MOSFET
UIS, Rg 100% Tested
Pb-Free Lead Plating & Halogen Free



•ABSOLUTE MAXIMUM RATINGS ($T_C = 25^{\circ}C$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNIT
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	$T_C = 25^{\circ}C$	103
		$T_C = 100^{\circ}C$	65
Continuous Drain Current	I_D	$T_A = 25^{\circ}C$	16
		$T_A = 70^{\circ}C$	13
Pulsed Drain Current ¹	I_{DM}	232	A
Avalanche Current	I_{AS}	65	
Avalanche Energy	E_{AS}	211	mJ
Repetitive Avalanche Energy ²	E_{AR}	106	
Power Dissipation	P_D	$T_C = 25^{\circ}C$	62.5
		$T_C = 100^{\circ}C$	25
Power Dissipation	P_D	$T_A = 25^{\circ}C$	1.7
		$T_A = 70^{\circ}C$	1.1
Operating Junction & Storage Temperature Range	T_j, T_{stg}	-55 to 150	$^{\circ}C$

•THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		2	$^{\circ}C/W$
Junction-to-Ambient ³	$R_{\theta JA}$		75	

¹Pulse width limited by maximum junction temperature.

²Duty cycle < 1%

³75 $^{\circ}C/W$ when mounted on a 1 in² pad of 2 oz copper.

⁴Guarantee by Engineering test

▪ ELECTRICAL CHARACTERISTICS (T_j = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage ⁴	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250uA	30			V
Gate Threshold Voltage ⁴	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250uA	1.2	1.6	2.5	
Gate-Body Leakage ⁴	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current ⁴	I _{DSS}	V _{DS} = 24V, V _{GS} = 0V			1	uA
		V _{DS} = 20V, V _{GS} = 0V, T _j = 125 °C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 10V, V _{GS} = 10V	103			A
Drain-Source On-State Resistance ^{1,4}	R _{DS(ON)}	V _{GS} = 10V, I _D = 24A		2.8	3.5	mΩ
		V _{GS} = 4.5V, I _D = 20A		3.7	5.0	
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 20A		25		S
DYNAMIC						
Input Capacitance ⁵	C _{iss}	V _{GS} = 0V, V _{DS} = 15V, f = 1MHz		2445		pF
Output Capacitance ⁵	C _{oss}			370		
Reverse Transfer Capacitance ⁵	C _{rss}			242		
Gate Resistance ^{4,5}	R _g	f = 1MHz		1.3		Ω
Total Gate Charge ^{1,2,5}	Q _g (V _{GS} =10V)	V _{DS} = 15V, V _{GS} = 10V, I _D = 24A		47.0		nC
	Q _g (V _{GS} =4.5V)			24.0		
Gate-Source Charge ^{1,2,5}	Q _{gs}			5.3		
Gate-Drain Charge ^{1,2,5}	Q _{gd}			10.6		
Turn-On Delay Time ^{1,2,5}	t _{d(on)}		V _{DS} = 15V, V _{GS} = 10V, I _D = 5A, R _g = 6Ω		10.6	
Rise Time ^{1,2,5}	t _r			18.0		
Turn-Off Delay Time ^{1,2,5}	t _{d(off)}			62.6		
Fall Time ^{1,2,5}	t _f			38.2		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I _S				103	A
Pulsed Current ³	I _{SM}				232	
Forward Voltage ^{1,4}	V _{SD}	I _F = I _S , V _{GS} = 0V			1.3	V
Reverse Recovery Time ⁵	t _{rr}	I _F = 24A, dI _F /dt = 100A / uS		13.8		nS
Reverse Recovery Charge ⁵	Q _{rr}			5.8		nC

¹Pulse test : Pulse Width ≤ 300 usec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

⁴Guarantee by FT test Item

⁵Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.

▪ TYPICAL CHARACTERISTICS

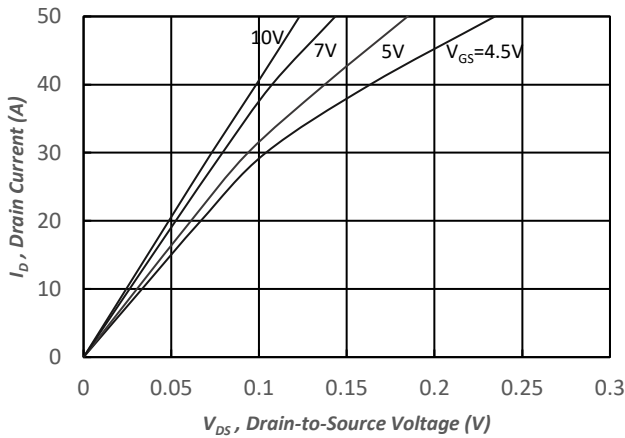


Fig.1 Typical Output Characteristics

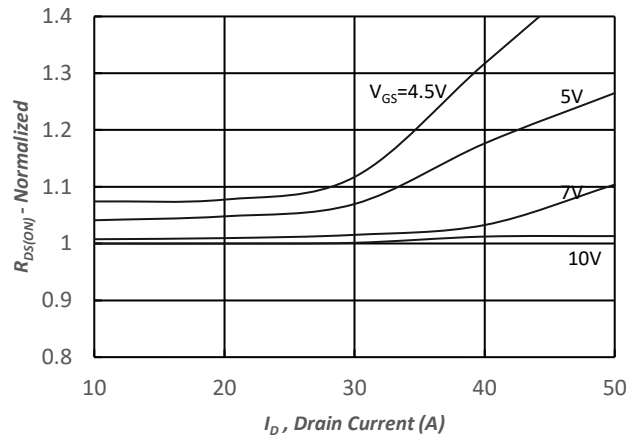


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

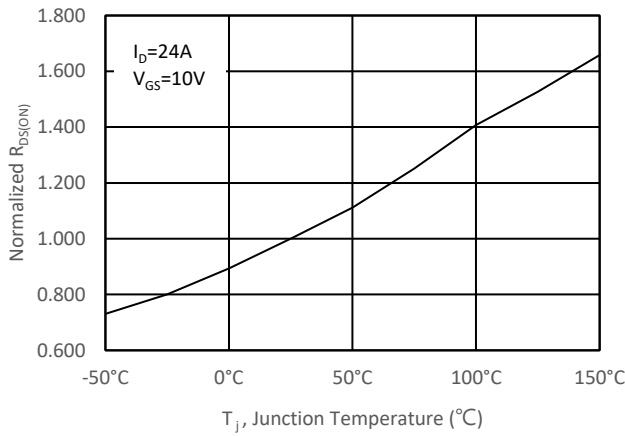


Fig.3 Normalized On-Resistance v.s. Junction Temperature

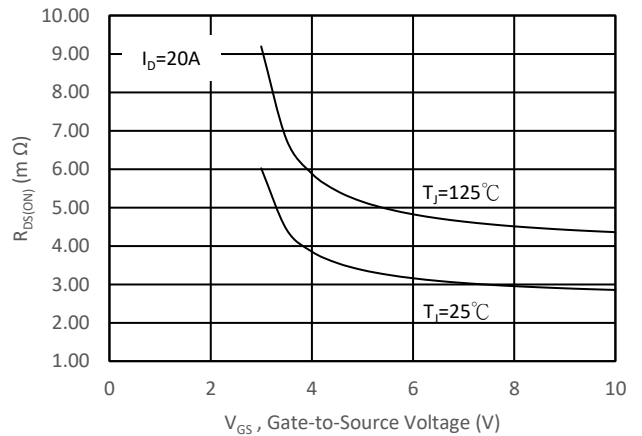


Fig.4 On-Resistance v.s. Gate Voltage

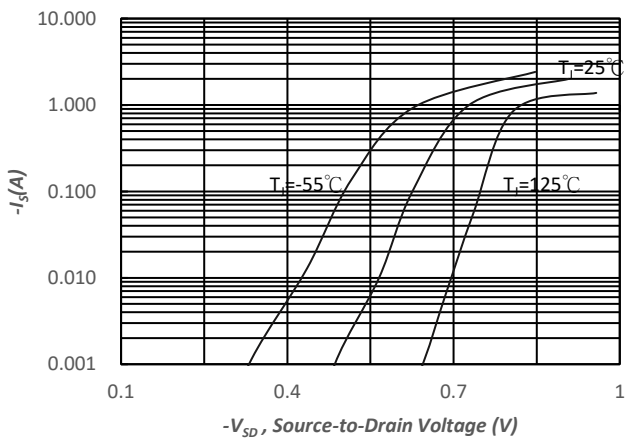


Fig.5 Forward Characteristic of Reverse Diode

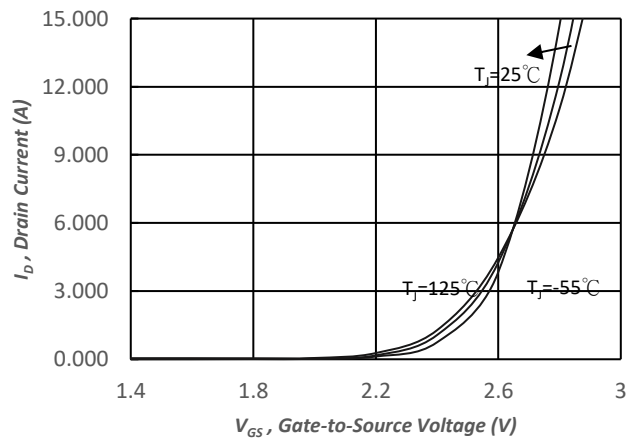


Fig.6 Transfer Characteristics

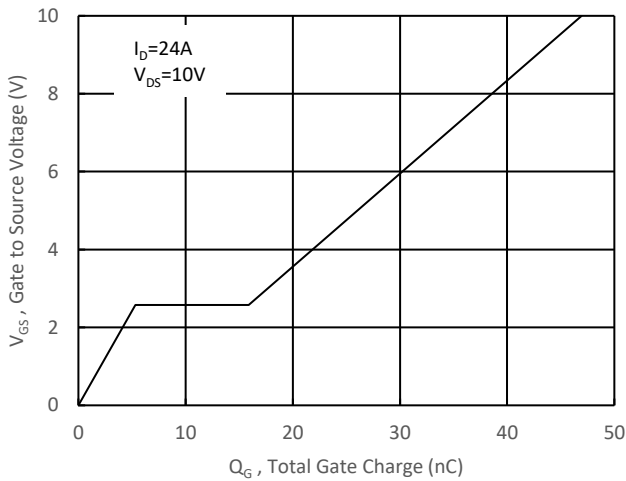


Fig.7 Gate Charge Characteristics

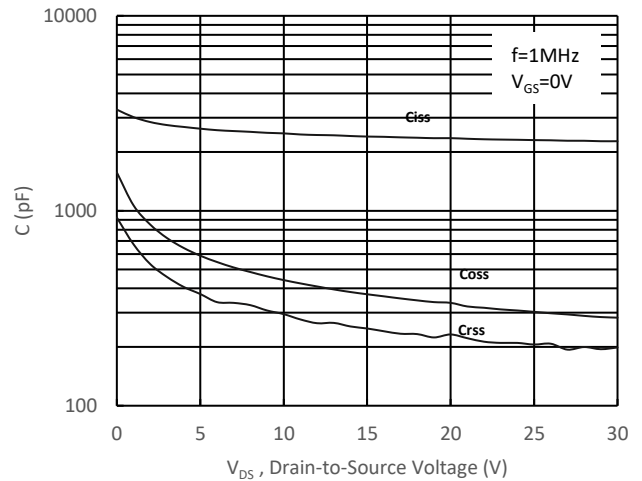


Fig.8 Typical Capacitance Characteristics

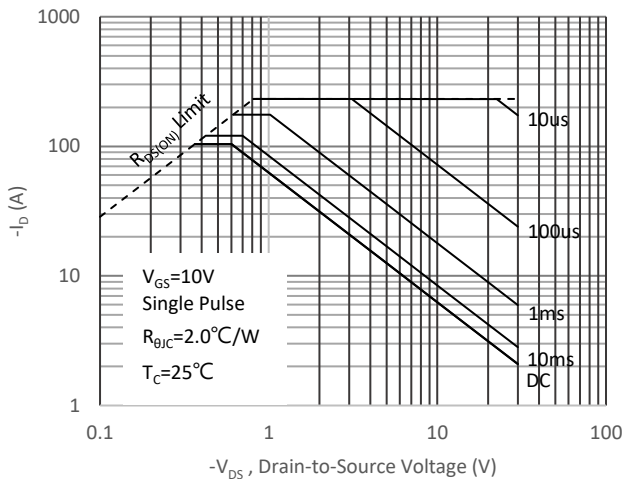


Fig.9. Maximum Safe Operating Area

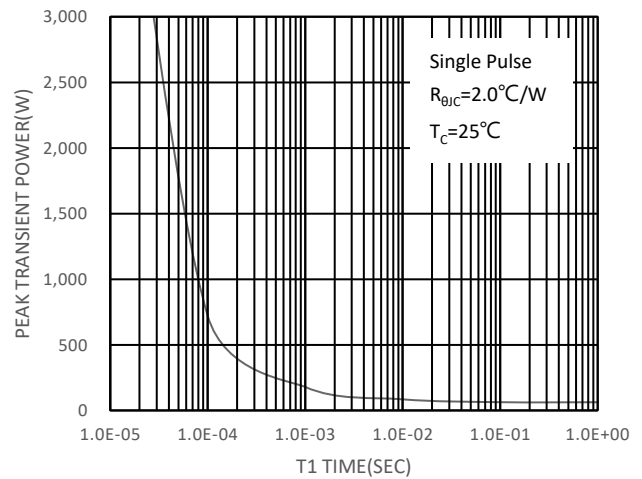


Fig.10. Single Pulse Maximum Power Dissipation

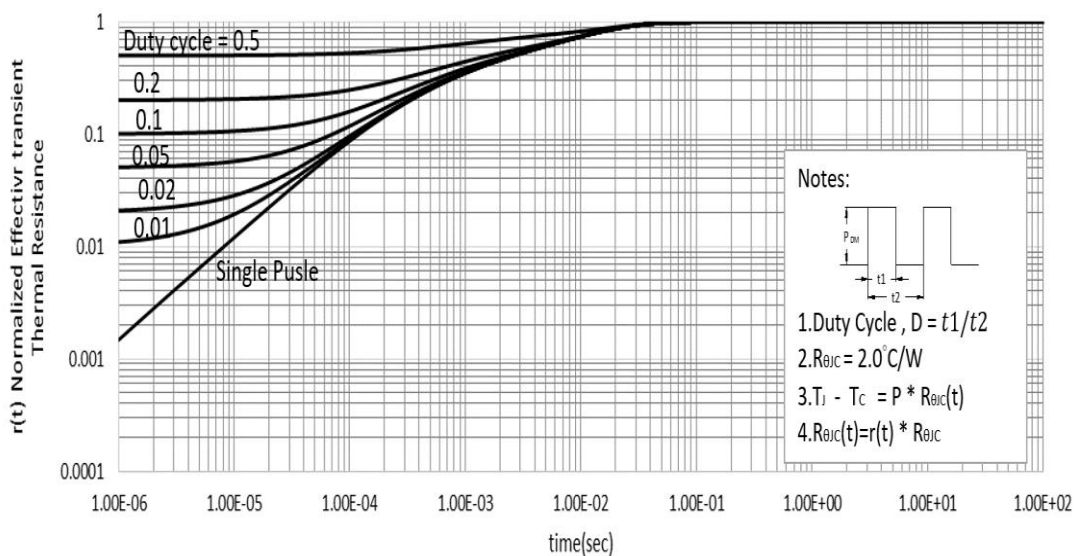


Fig.11. Effective Transient Thermal Impedance

Ordering & Marking Information:

Device Name: EMP31N03AQ for TO-252 (DPAK)



P31N03: Device Name

ABCDEFGH: Date Code

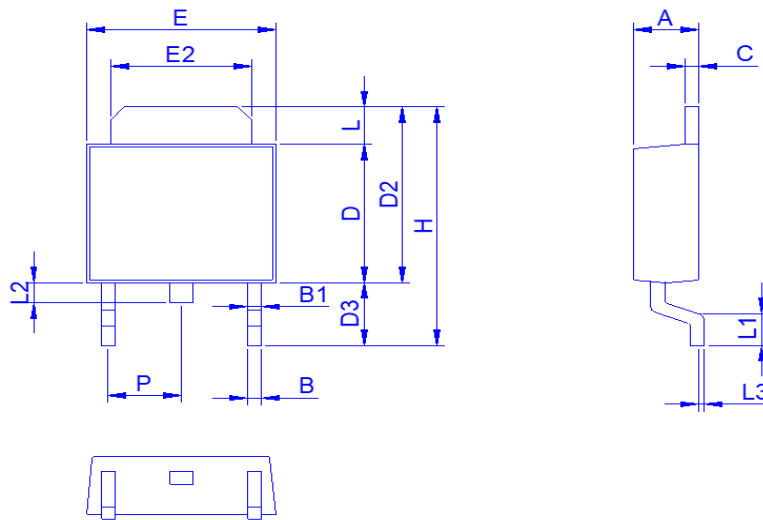
A: Assembly House

B: Year(A:2008 B:2009 C:2010....)

C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)

DEFG: Serial No.

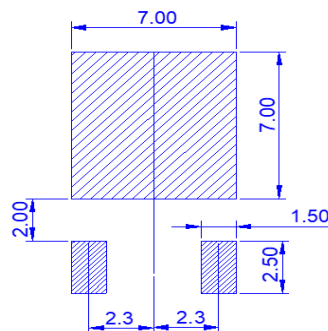
Outline Drawing



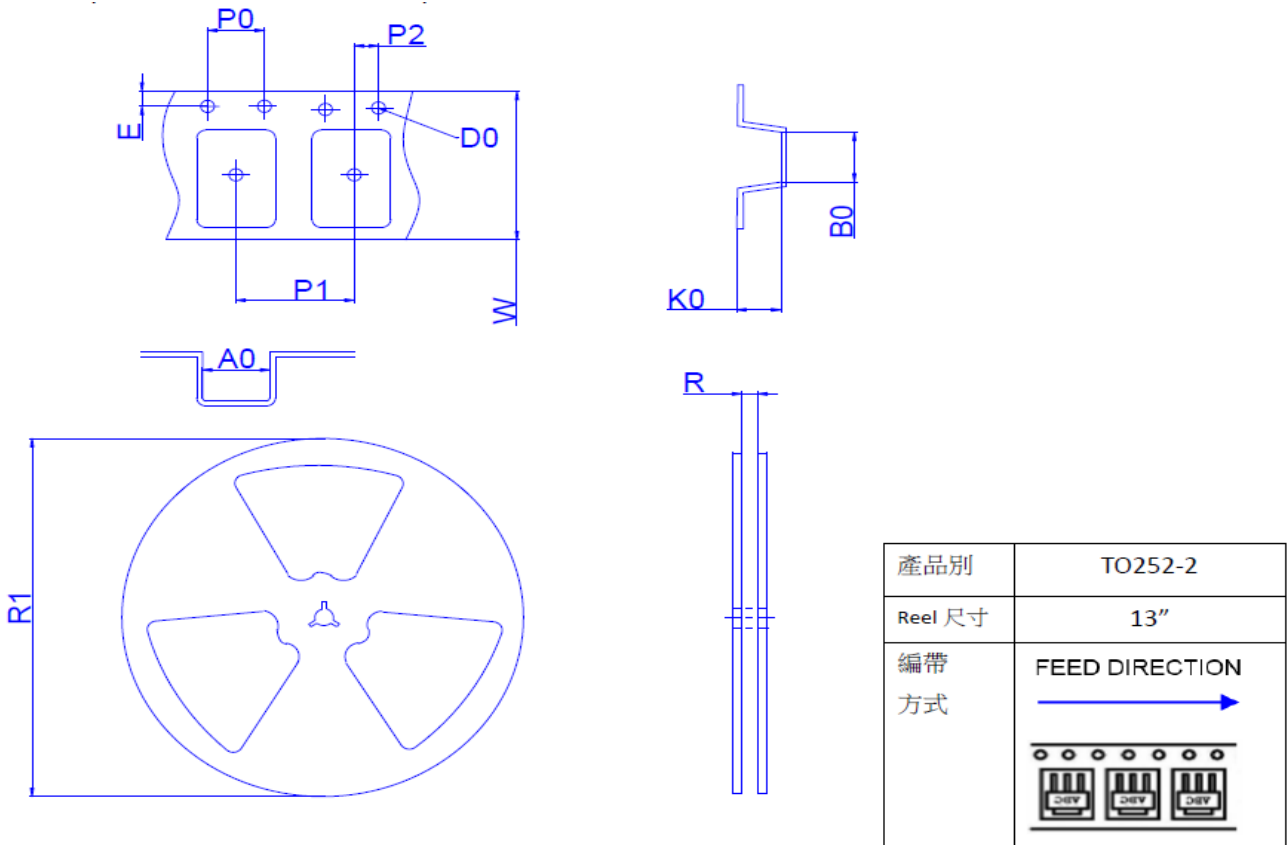
Dimension	A	B	B1	C	D	D2	D3	E	E2	H	L	L1	L2
Min.	2.1	0.62	0.65	0.45	5.96	6.8	2.6	6.3	4.9	9.3	0.8	1.2	0.5
Typ.	2.25	0.76	0.9	0.67	6.1	7.15	2.8	6.5	5.2	9.9	1.1	1.65	0.8
Max.	2.4	0.9	1.15	0.89	6.24	7.5	3	6.74	5.5	10.5	1.4	2.1	1.1

Dimension	L3	P
Min.	0	2.1
Typ.	0.1	2.25
Max.	0.2	2.4

Footprint



◆ Tape & Reel Information:2500pcs/Reel



Dimension in mm

Dimension	Carrier tape									Reel	
	A0	B0	D0	E	K0	P0	P1	P2	W	R	R1
Typ.	6.9	10.5	1.55	1.75	2.7	4	8	2	16	17	330
±	1	1	0.2	0.1	0.2	0.2	0.1	0.1	0.3	2	2