

P-Channel Logic Level Enhancement Mode Field Effect Transistor

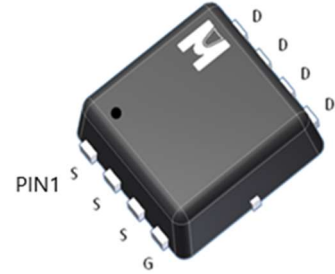
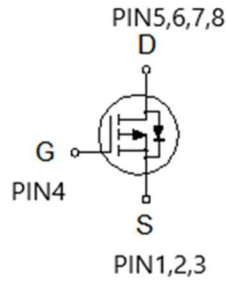
Product Summary:

BV_{DSS}	-20V
$R_{DS(on)}$ (MAX.)	100m Ω
I_D	-4.5A

P-Channel MOSFET

UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 12	V
Continuous Drain Current	$T_A = 25^\circ\text{C}$	I_D	-4.5	A
	$T_A = 70^\circ\text{C}$		-3.3	
Pulsed Drain Current ¹		I_{DM}	-18	
Power Dissipation	$T_A = 25^\circ\text{C}$	P_D	2.5	W
	$T_A = 70^\circ\text{C}$		1.6	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		6	$^\circ\text{C}/\text{W}$
Junction-to-Ambient ³	$R_{\theta JA}$		50	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$

³50 $^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper.



ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = -250μA	-20			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250μA	-0.3	-0.75	-1.2	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±12V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -16V, V _{GS} = 0V			-1	μA
		V _{DS} = -16V, V _{GS} = 0V, T _J = 125 °C			-10	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = -5V, V _{GS} = -4.5V	-4.5			A
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = -4.5V, I _D = -3.4A		83	100	mΩ
		V _{GS} = -2.5V, I _D = -2.5A		110	135	
		V _{GS} = -1.8V, I _D = -1A		140	180	
Forward Transconductance ¹	g _{fs}	V _{DS} = -5V, I _D = -3A		4.5		S
DYNAMIC						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = -10V, f = 1MHz		450		pF
Output Capacitance	C _{oss}			58		
Reverse Transfer Capacitance	C _{rss}			41		
Total Gate Charge ^{1,2}	Q _g	V _{DS} = -10V, V _{GS} = -4.5V, I _D = -3A		5.4		nC
Gate-Source Charge ^{1,2}	Q _{gs}			1.0		
Gate-Drain Charge ^{1,2}	Q _{gd}			1.3		
Turn-On Delay Time ^{1,2}	t _{d(on)}	V _{DS} = -10V, I _D = -1A, V _{GS} = -4.5V, R _{GS} = 6Ω		10		nS
Rise Time ^{1,2}	t _r			20		
Turn-Off Delay Time ^{1,2}	t _{d(off)}			15		
Fall Time ^{1,2}	t _f			12		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I _S				-4.5	A
Pulsed Current ³	I _{SM}				-18	
Forward Voltage ¹	V _{SD}	I _F = I _S , V _{GS} = 0V			-1.2	V

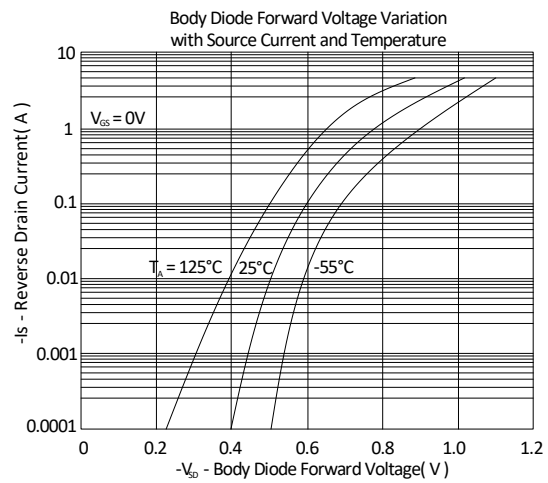
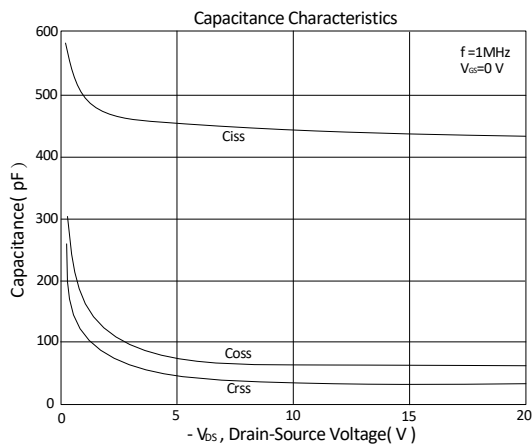
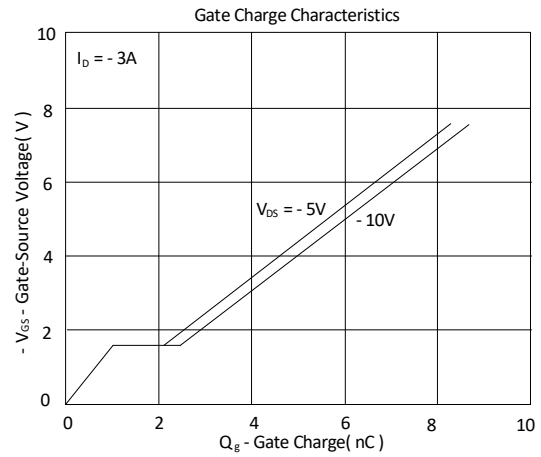
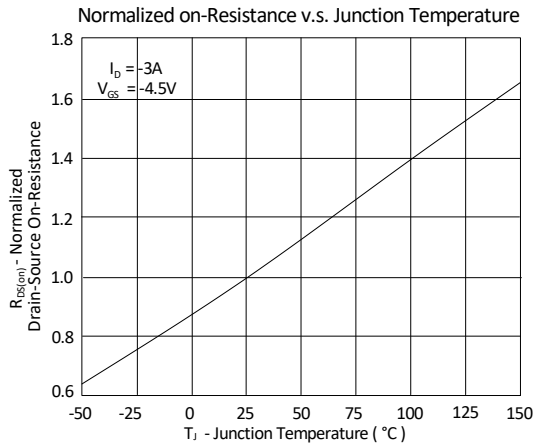
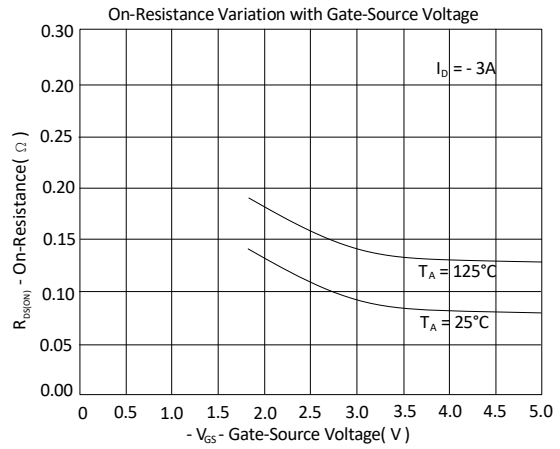
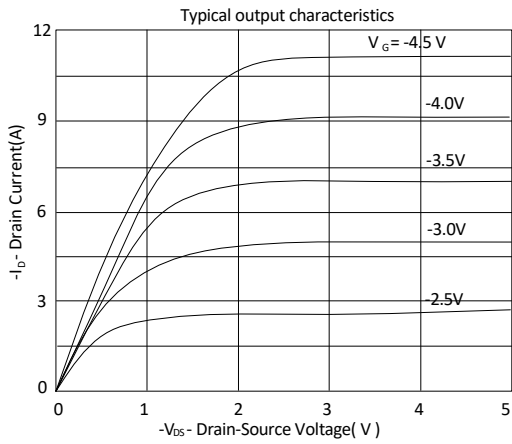
¹Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

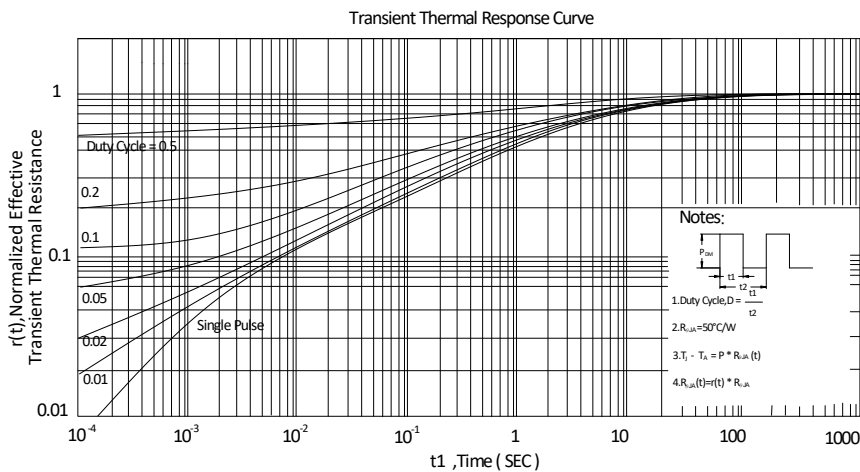
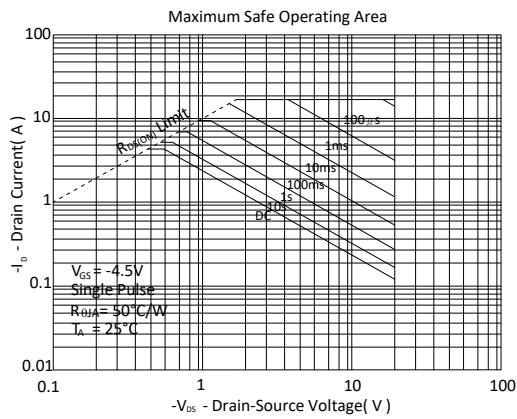
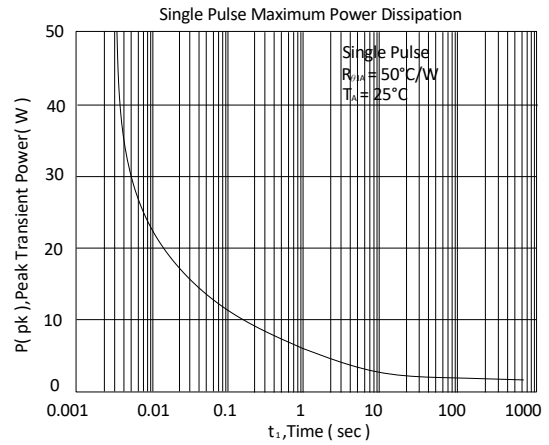
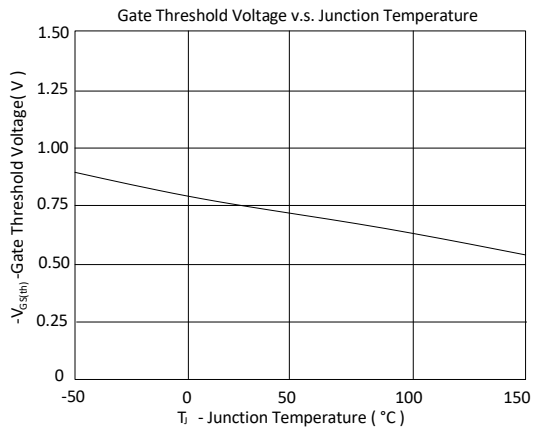
²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

EMC will review datasheet by quarter, and update new version.

TYPICAL CHARACTERISTICS





Ordering & Marking Information:

Device Name: EMFA0P02V for EDFN 3 x 3



FA0P02: Device Name

ABCDEFG: Date Code

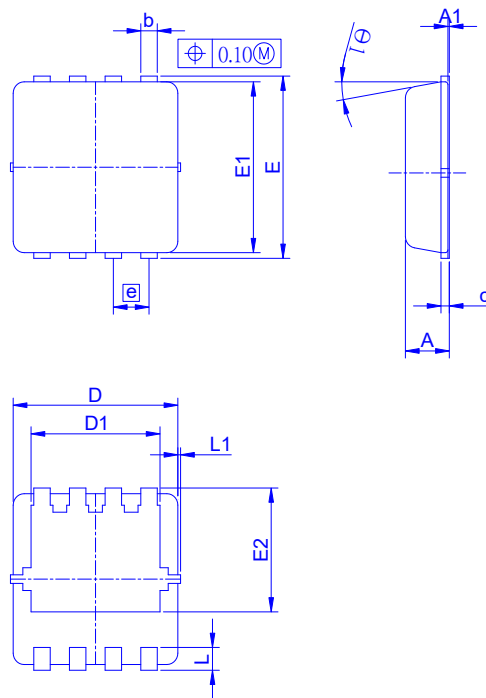
A: Assembly House

B: Year(A:2008 B:2009 C:2010...)

C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)

DEFG: Serial No.

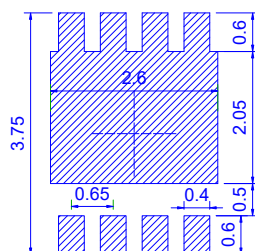
Outline Drawing



Dimension in mm

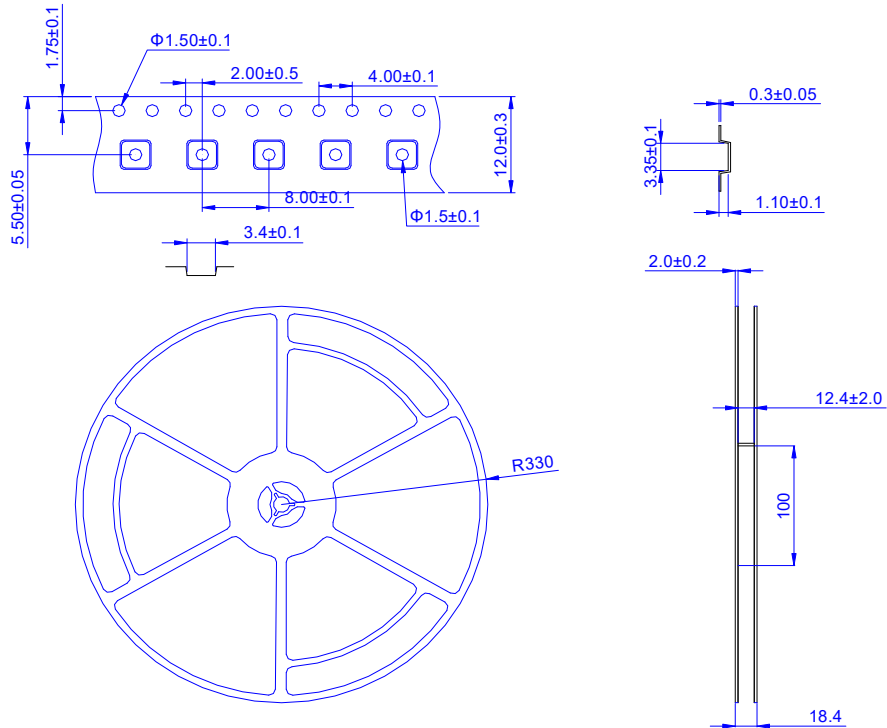
Dimension	A	A1	b	c	D	D1	E	E1	E2	e	L	L1	θ
Min.	0.65	0	0.20	0.10	2.90	2.15	3.10	2.90	1.53	0.55	0.25	-	0°
Typ.	0.75	-	0.30	0.15	3.00	2.45	3.20	3.00	1.97	0.65	0.40	0.075	10°
Max.	0.90	0.05	0.40	0.25	3.30	2.74	3.50	3.30	2.59	0.75	0.60	0.150	14°

Recommended minimum pads





Tape&Reel Information: 5000pcs/Reel



產品別	EDFN3X3
Reel 尺寸	13"
編帶方式	<p>FEEED DIRECTION</p>
前空格	50
後空格	50
裝箱數	
滿捲數量	5K
捲/內盒比	1 : 1
內盒滿箱數	5K
內/外箱比	10 : 1
外箱滿箱數	50K