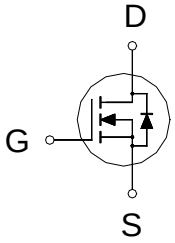
N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	20V
$R_{DSON\ (MAX.)}$	45mΩ
I_D	3.6A



Pb-Free Lead Plating & Halogen Free

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±12	V
Continuous Drain Current	T_A = 25 °C	I_D	3.6	A
	T_A = 70 °C		2.9	
Pulsed Drain Current[1]		I_{DM}	14	
Power Dissipation	T_A = 25 °C	P_D	1.04	W
	T_A = 70 °C		0.66	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Ambient[3]	$R_{\theta JA}$ (T ≤ 10sec)		83	°C / W
	$R_{\theta JA}$ (Steady State)		120	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle ≤ 1%

[3]The device mounted on a 1 in^2 pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

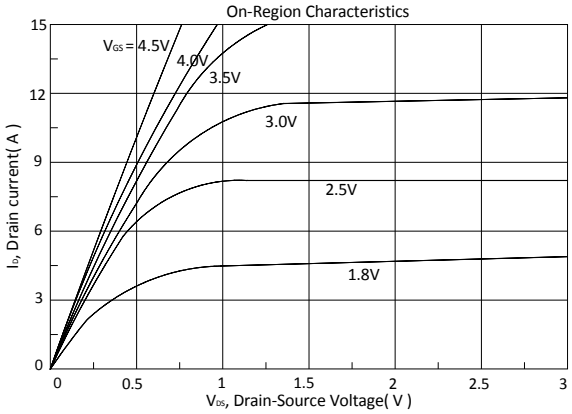
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	20			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	0.4	0.75	1.2	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±12V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 16V, V_{GS} = 0V			1	μA
		V_{DS} = 16V, V_{GS} = 0V, T_J = 125 °C			10	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 5V, V_{GS} = 10V	3.6			A
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = 4.5V, I_D = 3.5A		36	45	mΩ
		V_{GS} = 2.5V, I_D = 2A		43	60	
		V_{GS} = 1.8V, I_D = 1A		58	85	
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 3.5A		5		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 10V, f = 1MHz		355		pF
Output Capacitance	C_{oss}			56		
Reverse Transfer Capacitance	C_{rss}			40		
Total Gate Charge[1,2]	Q_g	V_{DS} = 10V, V_{GS} = 4.5V, I_D = 3.5A		4.6		nC
Gate-Source Charge[1,2]	Q_{gs}			0.66		
Gate-Drain Charge[1,2]	Q_{gd}			1.5		
Turn-On Delay Time[1,2]	$t_{d(on)}$	V_{DS} = 10V, I_D = 1A, V_{GS} = 4.5V, R_{GS} = 6Ω		8		nS
Rise Time[1,2]	t_r			10		
Turn-Off Delay Time[1,2]	$t_{d(off)}$			20		
Fall Time[1,2]	t_f			15		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I_S				2	A
Pulsed Current[3]	I_{SM}				8	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0V			1.2	V

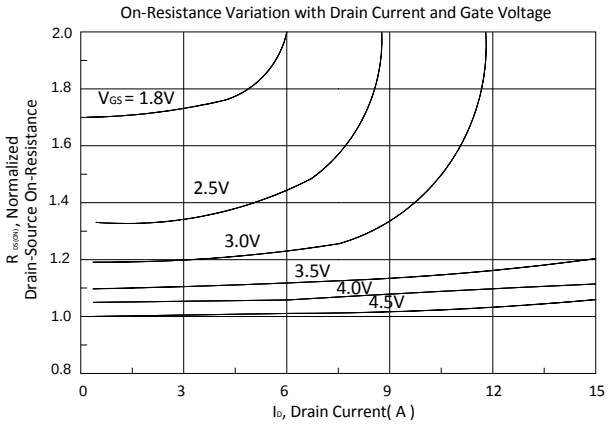
[1]Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

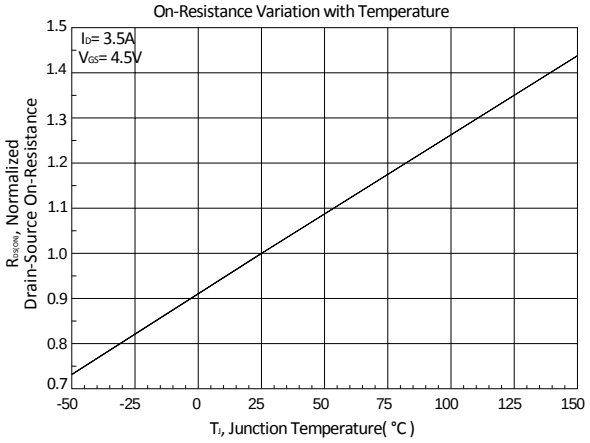
[2]Independent of operating temperature.

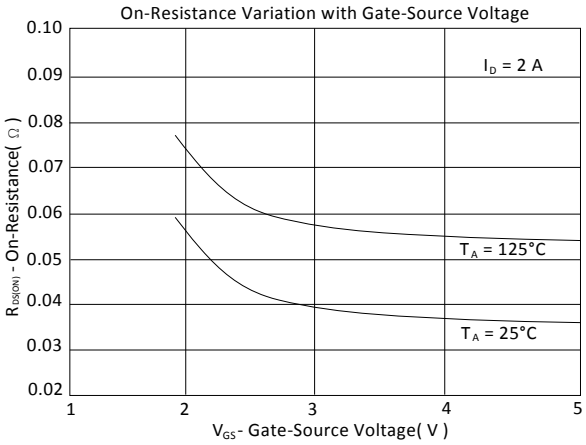
[3]Pulse width limited by maximum junction temperature.

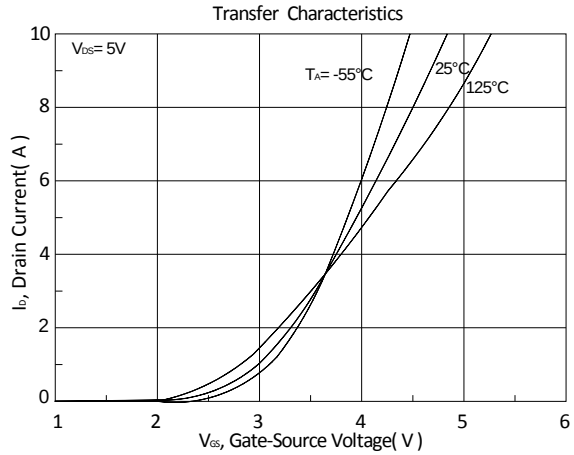
TYPICAL CHARACTERISTICS

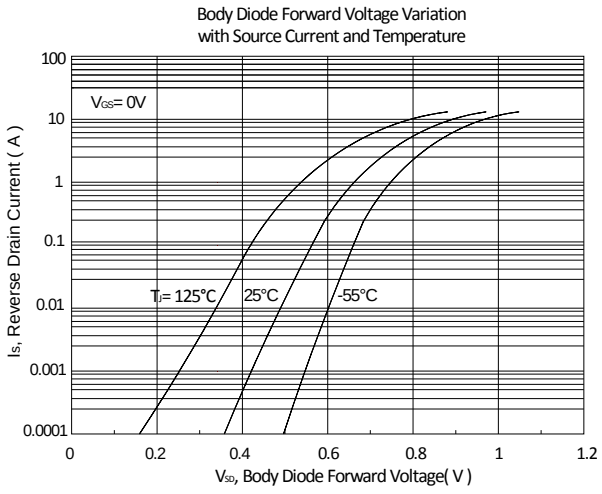


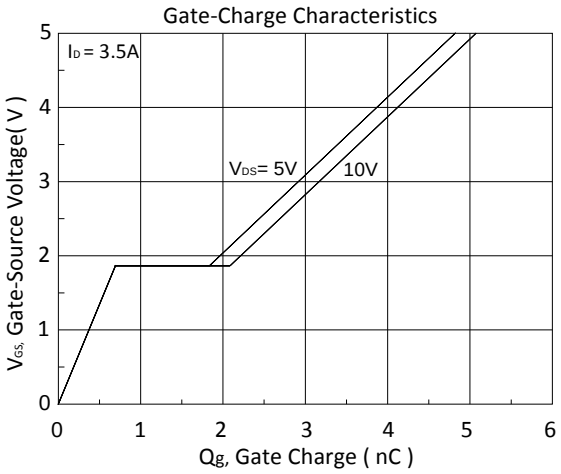


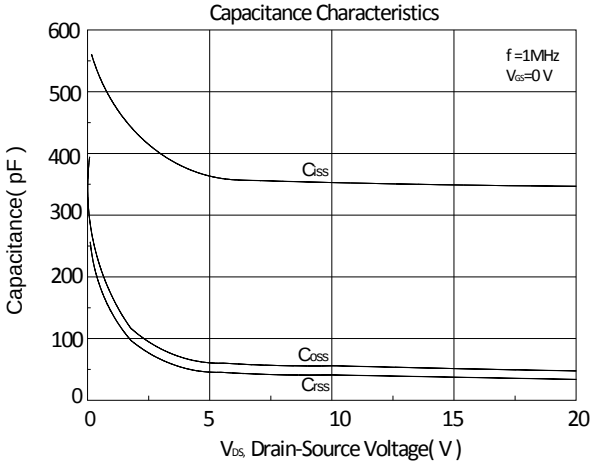


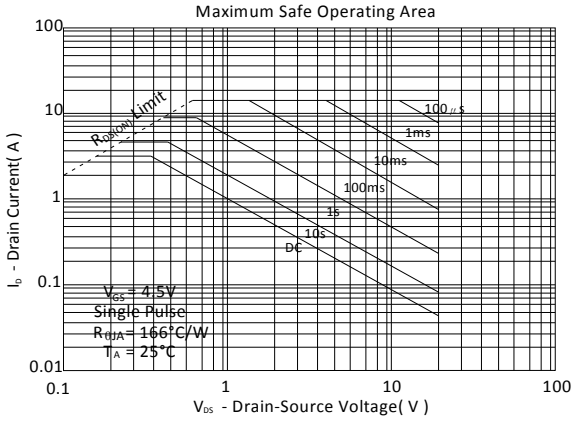


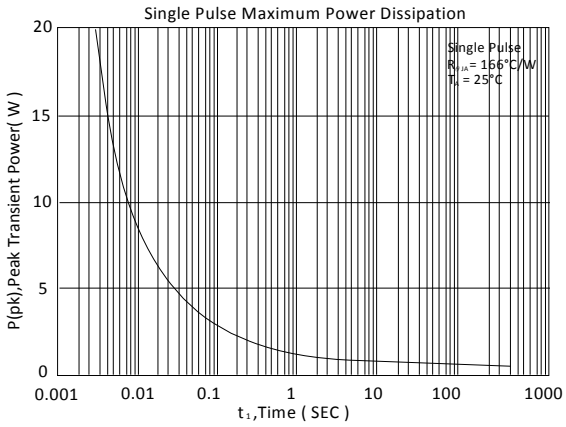


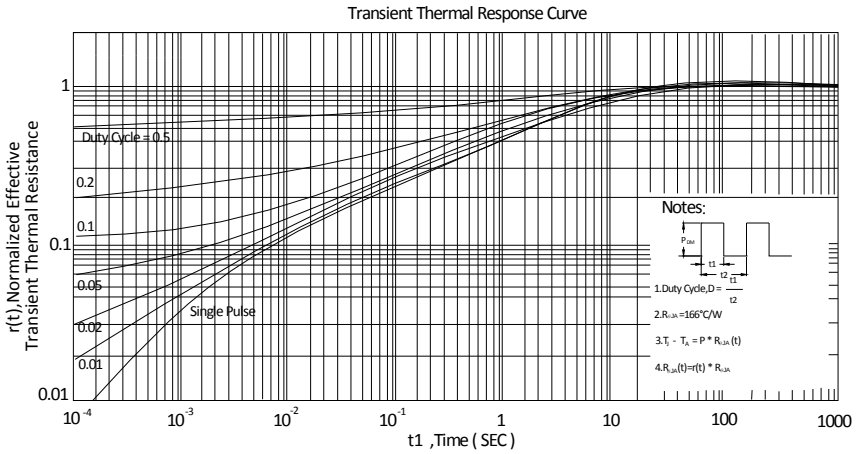



Gate-Charge Characteristics
I_D = 3.5A
V_{DS}= 5V
10V
V_{GS}, Gate-Source Voltage(V)
Qg, Gate Charge (nC)


Capacitance Characteristics
f =1MHz
V_{GS}=0 V
Ciss
Coss
Crss
Capacitance(pF)
V_{DS}, Drain-Source Voltage(V)

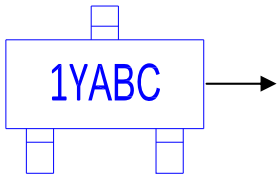

Maximum Safe Operating Area
$R_{DS(ON)}$ Limit
100 μs
1ms
10ms
100ms
1s
10s
DC
V_{GS} = 4.5V
Single Pulse
$R_{\theta JA}$= 166°C/W
T_A = 25°C
I_D - Drain Current(A)
V_{DS} - Drain-Source Voltage(V)


Single Pulse Maximum Power Dissipation
Single Pulse
$R_{\theta JA}$= 166°C/W
T_A = 25°C
P(pk),Peak Transient Power(W)
t_1,Time (SEC)


Transient Thermal Response Curve
Duty Cycle = 0.5
0.2
0.1
0.05
0.02
0.01
Single Pulse
Notes:
1.Duty Cycle,D =
2.$R_{\theta JA}$ =166°C/W
3.T_j - T_A = P * $R_{\theta JA}$(t)
4.$R_{\theta JA}$(t)=r(t) * $R_{\theta JA}$
r(t),Normalized Effective Transient Thermal Resistance
t1 ,Time (SEC)

Ordering & Marking Information:

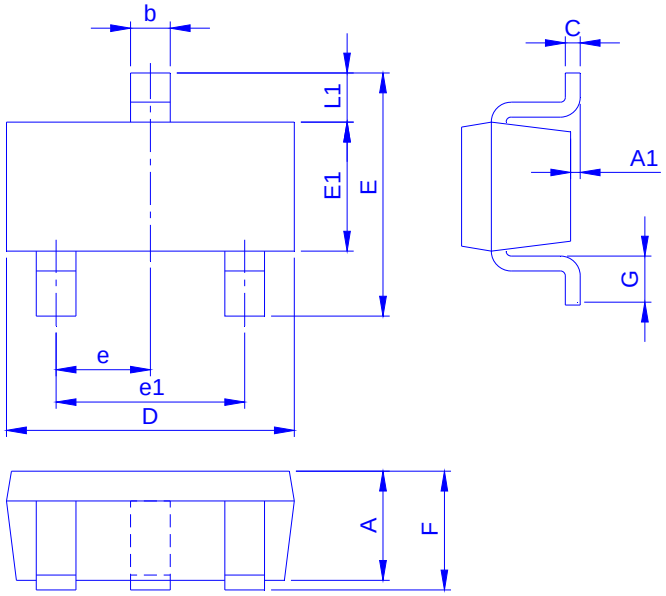
Device Name: EMF50N02JS for SOT-23



1Y: Device Code, 1Y for EMF50N02JS

ABC: Date Code

Outline Drawing



Dimension in mm

Dimension	A	A1	b	C	D	E	E1	e	e1	F	G	L1
Min.	0.70	0	0.3	0.08	2.80	2.25	1.2	0.90		0.80	0.3	0.50
Typ.					2.90			0.95	1.9			
Max.	1.15	0.1	0.5	0.20	3.02	3.00	1.7	1.00		1.25	0.6	0.75

Footprint