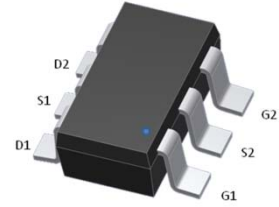
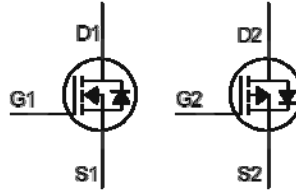


N & P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

	N-CH	P-CH
BV_{DSS}	20V	-20V
$R_{DS(on) (MAX.)}$	30.5m Ω	100m Ω
I_D	5A	-3.2A



Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS		UNIT
Gate-Source Voltage		V_{GS}	N-CH	P-CH	V
			± 12	± 12	
Continuous Drain Current	$T_A = 25^\circ\text{C}$	I_D	5	-3.2	A
	$T_A = 100^\circ\text{C}$		3.5	-2.5	
Pulsed Drain Current ¹		I_{DM}	20	-12.8	
Power Dissipation	$T_A = 25^\circ\text{C}$	P_D	1.25		W
	$T_A = 70^\circ\text{C}$		0.8		
Operating Junction & Storage Temperature Range		T_{j}, T_{stg}	-55 to 150		$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Ambient	$R_{\theta JA}$		100	$^\circ\text{C} / \text{W}$

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$



ELECTRICAL CHARACTERISTICS ($T_c = 25\text{ }^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT	
			MIN	TYP	MAX		
STATIC							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$ $V_{GS} = 0V, I_D = -250\mu A$	N-CH	20			V
			P-CH	-20			
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$ $V_{DS} = V_{GS}, I_D = -250\mu A$	N-CH	0.4	0.75	1.2	
			P-CH	-0.4	-0.75	-1.2	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 12V$ $V_{DS} = 0V, V_{GS} = \pm 12V$	N-CH			± 100	nA
			P-CH			± 100	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 16V, V_{GS} = 0V$ $V_{DS} = -16V, V_{GS} = 0V$	N-CH			1	μA
			P-CH			-1	
			N-CH			10	
			P-CH			-10	
On-State Drain Current ¹	$I_{D(ON)}$	$V_{DS} = 5V, V_{GS} = 4.5V$ $V_{DS} = -5V, V_{GS} = -4.5V$	N-CH	5			A
			P-CH	-3.2			
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = 4.5V, I_D = 5A$ $V_{GS} = -4.5V, I_D = -3A$ $V_{GS} = 2.5V, I_D = 3A$ $V_{GS} = -2.5V, I_D = -1A$	N-CH		26	30.5	m Ω
			P-CH		85	100	
			N-CH		40	50	
			P-CH		120	150	
Forward Transconductance ¹	g_{fs}	$V_{DS} = 5V, I_D = 5A$ $V_{DS} = -5V, I_D = -3A$	N-CH		7		S
			P-CH		4.5		
DYNAMIC							
Input Capacitance	C_{iss}	N-CH $V_{GS} = 0V, V_{DS} = 15V, f = 1MHz$	N-CH		280		pF
			P-CH		382		
Output Capacitance	C_{oss}	P-CH $V_{GS} = 0V, V_{DS} = -15V, f = 1MHz$	N-CH		47		
			P-CH		70		
Reverse Transfer Capacitance	C_{rss}		N-CH		38		
			P-CH		60		
Gate Resistance	R_g	$V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz$	N-CH		2.0		Ω
			P-CH		5.0		



Total Gate Charge ^{1,2}	Q_g	N-CH $V_{DS} = 10V, V_{GS} = 4.5V,$ $I_D = 5A$ P-CH $V_{DS} = -10V, V_{GS} = -4.5V,$ $I_D = -3A$	N-CH		6.2		nC	
Gate-Source Charge ^{1,2}	Q_{gs}		P-CH		7.2			
Gate-Drain Charge ^{1,2}	Q_{gd}		N-CH		0.9			
			P-CH		1.2			
Turn-On Delay Time ^{1,2}	$t_{d(on)}$		N-CH		5			nS
			P-CH		5			
Rise Time ^{1,2}	t_r	$I_D = 1A, V_{GS} = 4.5V, R_{GS} = 6\Omega$	N-CH		10			
Turn-Off Delay Time ^{1,2}	$t_{d(off)}$		P-CH		20			
Fall Time ^{1,2}	t_f	$I_D = -1A, V_{GS} = -4.5V, R_{GS} = 6\Omega$	N-CH		8			
			P-CH		10			
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_c = 25\text{ }^\circ\text{C}$)								
Continuous Current	I_S		N-CH			2	A	
			P-CH			-2		
Pulsed Current ³	I_{SM}		N-CH			8		
			P-CH			-8		
Forward Voltage ¹	V_{SD}		$I_F = I_S, V_{GS} = 0V$	N-CH			1.3	V
				P-CH			-1.3	

¹Pulse test : Pulse Width $\leq 300\ \mu\text{sec}$, Duty Cycle $\leq 2\%$.

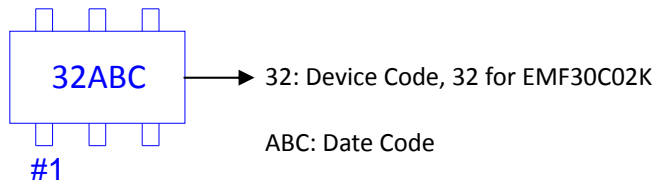
²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

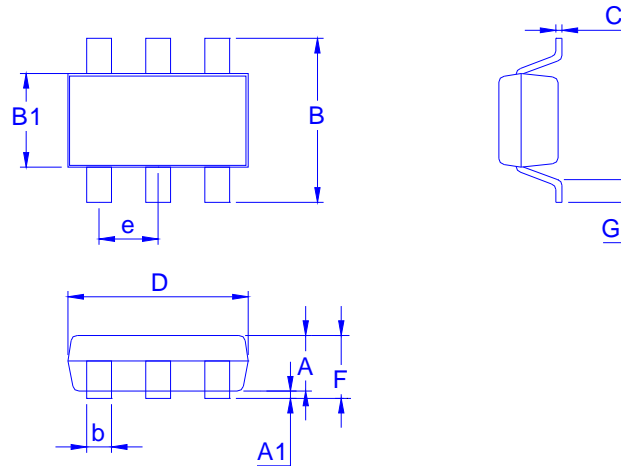


Ordering & Marking Information:

Device Name: EMF30C02K for TSOP-6



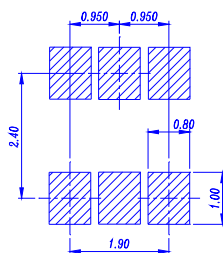
Outline Drawing



Dimension in mm

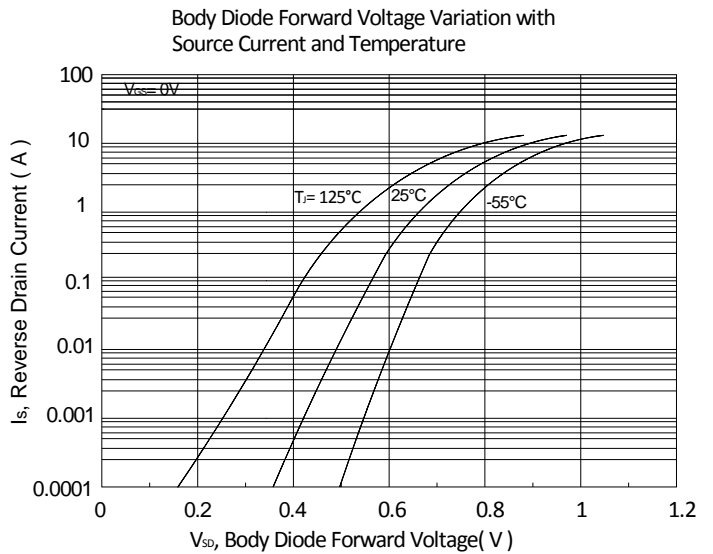
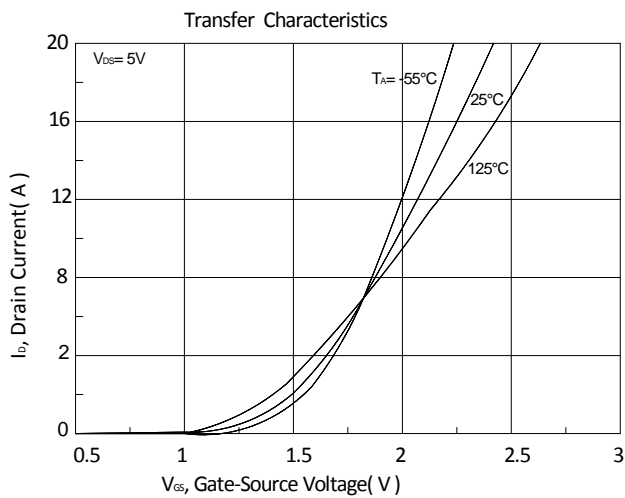
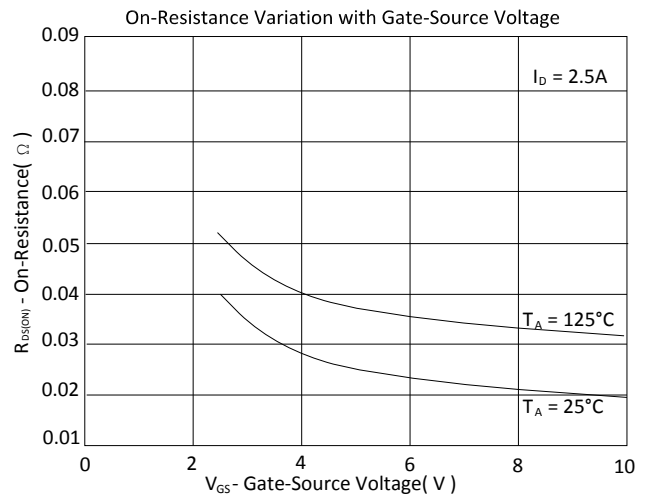
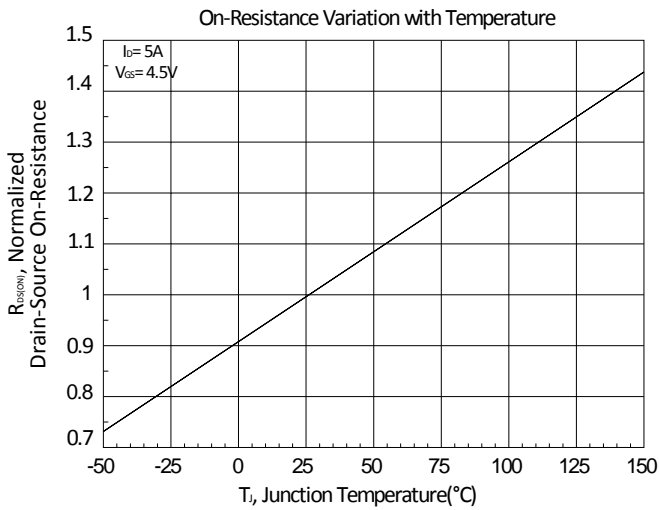
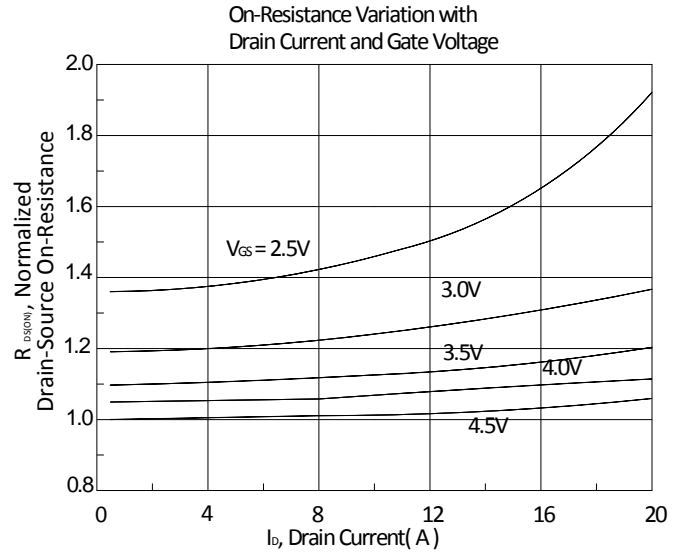
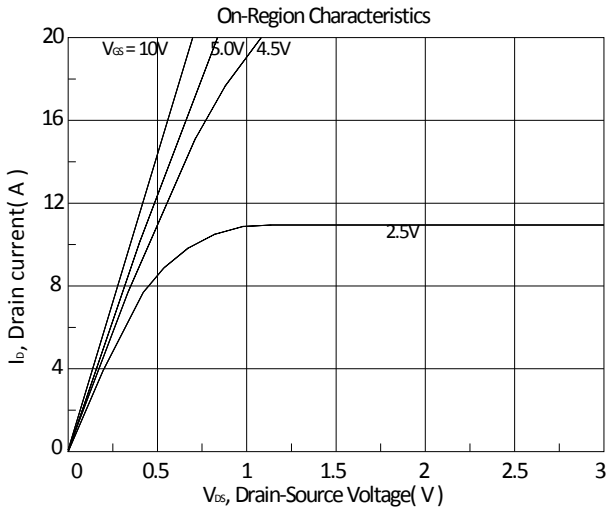
Dimension	A	A1	B	B1	b	C	D	e	F	G
Min.	0.85	0	2.50	1.50	0.30	0.08	2.70		0.85	0.20
Typ.	0.95		2.80	1.60	0.40		2.90	0.95		
Max.	1.25	0.15	3.10	1.70	0.50	0.20	3.10		1.40	0.60

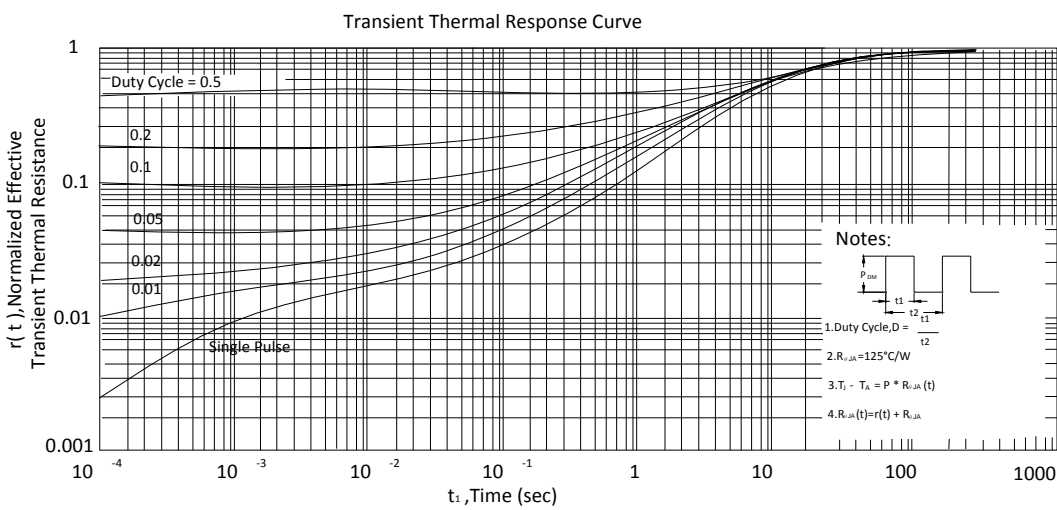
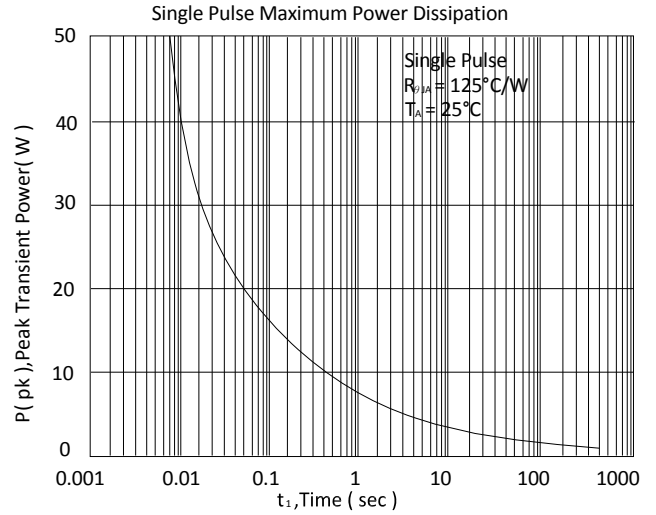
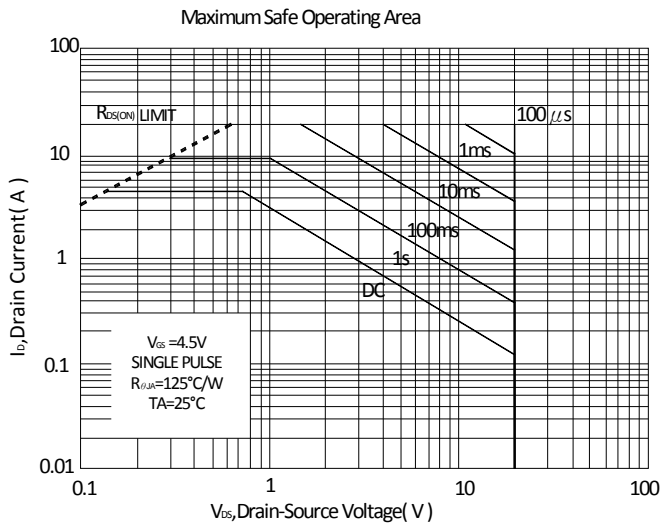
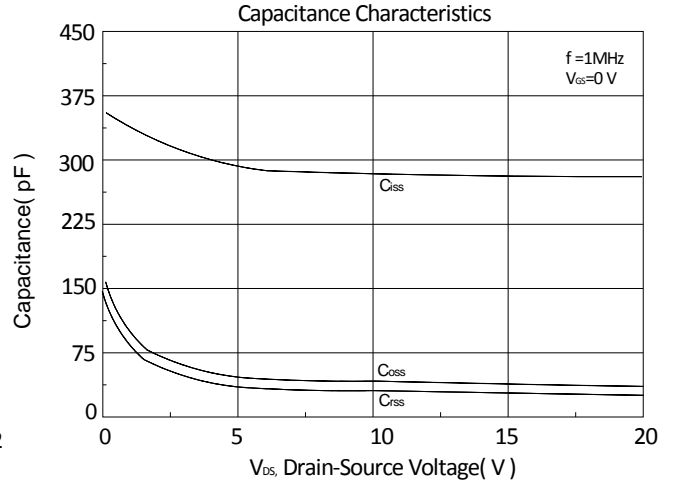
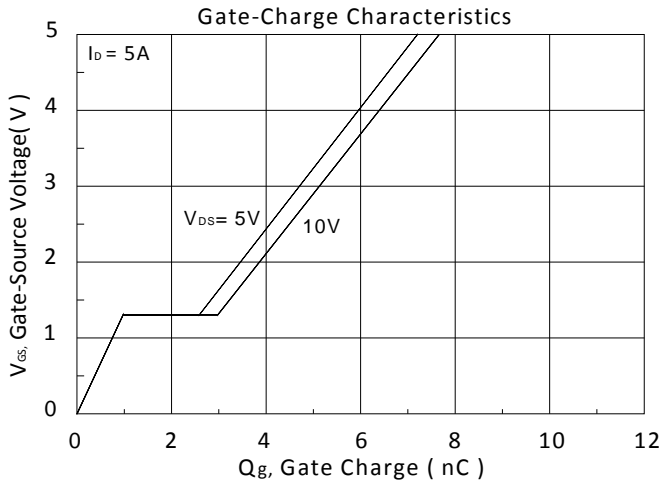
Footprint





N-Channel







P-Channel

