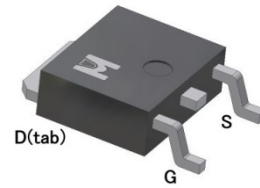


P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	-20V
$R_{DS(on)}$ (MAX.)	9m Ω
I_D	-62A



Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 8	V
Continuous Drain Current	$T_C = 25\text{ }^\circ\text{C}$	I_D	-62	A
	$T_C = 100\text{ }^\circ\text{C}$		-41	
Pulsed Drain Current ¹		I_{DM}	-150	
Avalanche Current		I_{AS}	-25	
Avalanche Energy	$L = 0.1\text{mH}$, $I_D = -25\text{A}$, $R_G = 25\Omega$	E_{AS}	62.5	mJ
Repetitive Avalanche Energy ²	$L = 0.05\text{mH}$	E_{AR}	31.25	
Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	P_D	56	W
	$T_C = 100\text{ }^\circ\text{C}$		22	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		2.2	$^\circ\text{C} / \text{W}$
Junction-to-Ambient ³	$R_{\theta JA}$		62.5	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$



ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-20			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-0.4	-0.75	-1.2	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 8V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -16V, V_{GS} = 0V$			-1	μA
		$V_{DS} = -12V, V_{GS} = 0V, T_J = 125\text{ }^\circ\text{C}$			-10	
On-State Drain Current ¹	$I_{D(ON)}$	$V_{DS} = -5V, V_{GS} = -4.5V$	-62			A
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = -4.5V, I_D = -24A$		7.2	9	$m\Omega$
		$V_{GS} = -2.5V, I_D = -15A$		9.6	12.5	
		$V_{GS} = -1.8V, I_D = -5A$		14.5	18	
Forward Transconductance ¹	g_{fs}	$V_{DS} = -5V, I_D = -24A$		32		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = -10V, f = 1MHz$		7660		pF
Output Capacitance	C_{oss}			596		
Reverse Transfer Capacitance	C_{rss}			510		
Gate Resistance	R_g	$V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz$		3.0		Ω
Total Gate Charge ^{1,2}	$Q_g(V_{GS}=-4.5V)$	$V_{DS} = -10V, V_{GS} = -4.5V,$ $I_D = -24A$		51		nC
	$Q_g(V_{GS}=-2.5V)$			32		
Gate-Source Charge ^{1,2}	Q_{gs}			4.9		
Gate-Drain Charge ^{1,2}	Q_{gd}			13		
Turn-On Delay Time ^{1,2}	$t_{d(on)}$		$V_{DS} = -10V,$ $I_D = -1A, V_{GS} = -4.5V, R_{GS} = 6\Omega$		25	
Rise Time ^{1,2}	t_r			55		
Turn-Off Delay Time ^{1,2}	$t_{d(off)}$			150		
Fall Time ^{1,2}	t_f			65		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_C = 25\text{ }^\circ\text{C}$)						
Continuous Current	I_S				-62	A
Pulsed Current ³	I_{SM}				-150	
Forward Voltage ¹	V_{SD}	$I_F = -24A, V_{GS} = 0V$			-1.2	V

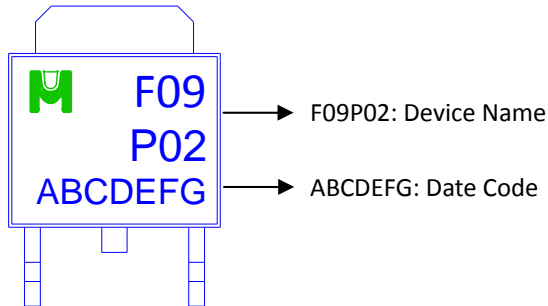
¹Pulse test : Pulse Width $\leq 300\ \mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

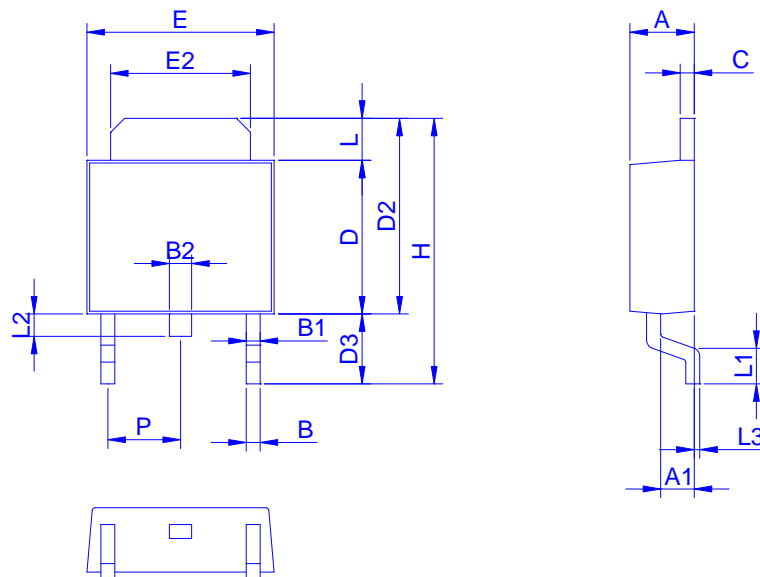
³Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: EMF09P02A for DPAK (TO-252)



Outline Drawing



Dimension in mm

Dimension	A	A1	B	B1	B2	C	D	D2	D3	E	E2	H	L	L1	L2	L3	P
Min.	2.10	0.95	0.30	0.40	0.60	0.40	5.30	6.70	2.20	6.40	4.80	9.20	0.89	0.90	0.50	0.00	2.10
Max.	2.50	1.30	0.85	0.94	1.00	0.60	6.20	7.30	3.00	6.70	5.45	10.15	1.70	1.65	1.10	0.30	2.50



TYPICAL CHARACTERISTICS

