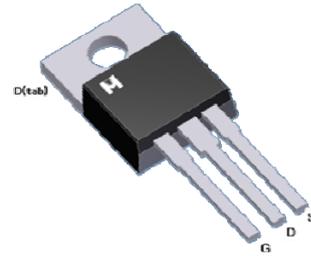
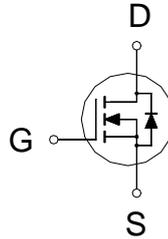


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	100V
$R_{DS(on)}$ (MAX.)	14m Ω
I_D	85A



UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 30	V
Continuous Drain Current	$T_C = 25\text{ }^\circ\text{C}$	I_D	85	A
	$T_C = 100\text{ }^\circ\text{C}$		60	
Pulsed Drain Current ¹		I_{DM}	250	
Avalanche Current		I_{AS}	40	
Avalanche Energy	$L = 0.1\text{mH}, I_{AS}=40\text{A}, R_G=25\Omega$	E_{AS}	80	mJ
Repetitive Avalanche Energy ²	$L = 0.05\text{mH}$	E_{AR}	40	
Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	P_D	147	W
	$T_C = 100\text{ }^\circ\text{C}$		58	
Operating Junction & Storage Temperature Range		T_{j}, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		0.85	$^\circ\text{C} / \text{W}$
Junction-to-Ambient	$R_{\theta JA}$		62.5	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	100			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	2.0	3.0	4.0	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±30V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 80V, V _{GS} = 0V			1	μA
		V _{DS} = 70V, V _{GS} = 0V, T _J = 125 °C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 10V, V _{GS} = 10V	85			A
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = 10V, I _D = 40A		12	14	mΩ
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 20A		42		S
DYNAMIC						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = 25V, f = 1MHz		6557		pF
Output Capacitance	C _{oss}			417		
Reverse Transfer Capacitance	C _{rss}			122		
Gate Resistance	R _g	V _{GS} = 15mV, V _{DS} = 0V, f = 1MHz		1.5		Ω
Total Gate Charge ^{1,2}	Q _g	V _{DS} = 50V, V _{GS} = 10V, I _D = 20A		64.7		nC
Gate-Source Charge ^{1,2}	Q _{gs}			24.4		
Gate-Drain Charge ^{1,2}	Q _{gd}			18.1		
Turn-On Delay Time ^{1,2}	t _{d(on)}	V _{DS} = 50V, I _D = 1A, V _{GS} = 10V, R _{GS} = 6Ω		25		nS
Rise Time ^{1,2}	t _r			120		
Turn-Off Delay Time ^{1,2}	t _{d(off)}			100		
Fall Time ^{1,2}	t _f			150		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I _S				85	A
Pulsed Current ³	I _{SM}				250	
Forward Voltage ¹	V _{SD}	I _F = 20A, V _{GS} = 0V			1.3	V
Reverse Recovery Time	t _{rr}	I _F = 25A, dI _F /dt = 100A / μS		150		nS
Reverse Recovery Charge	Q _{rr}				450	

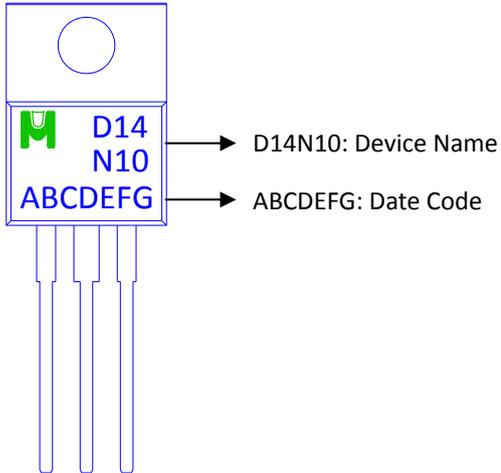
¹Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

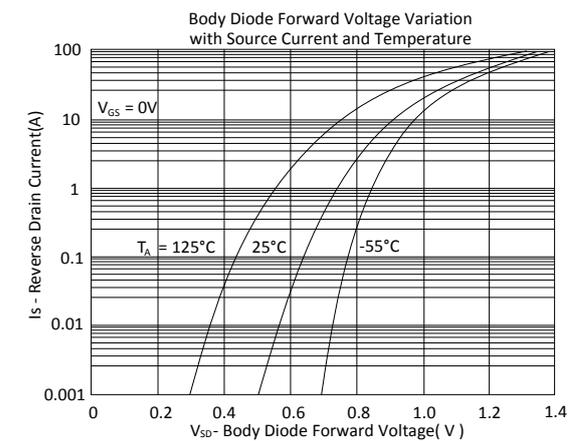
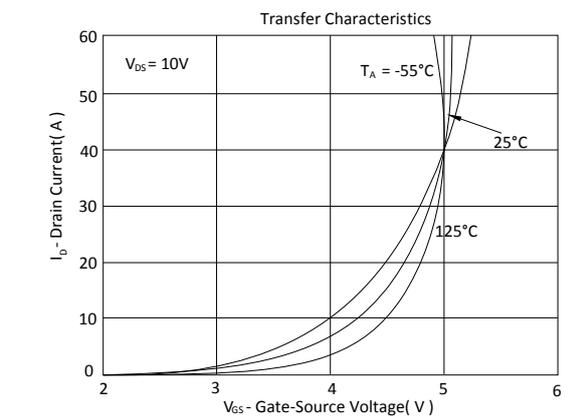
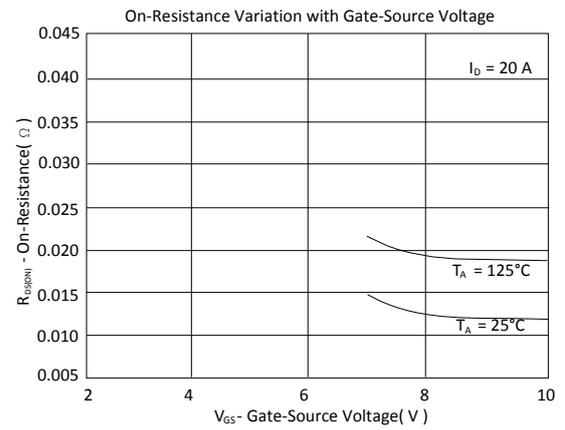
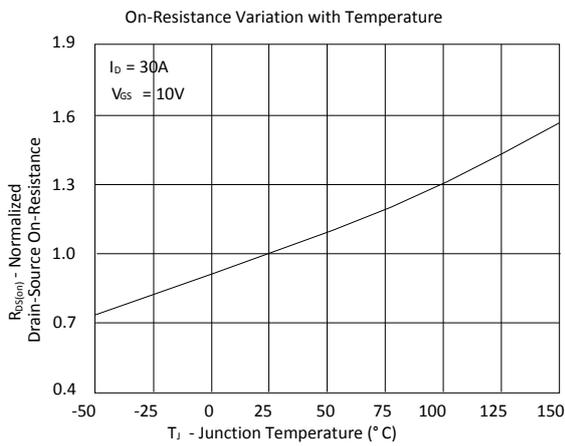
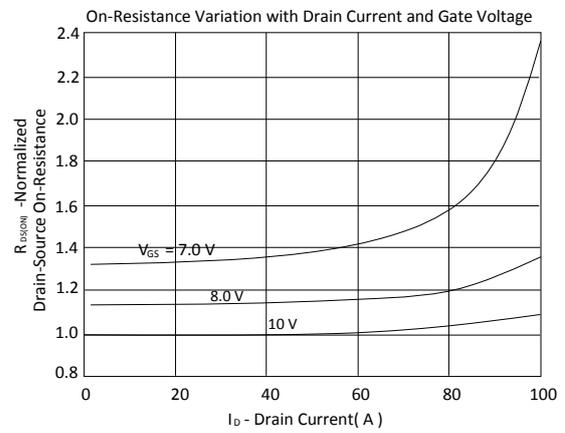
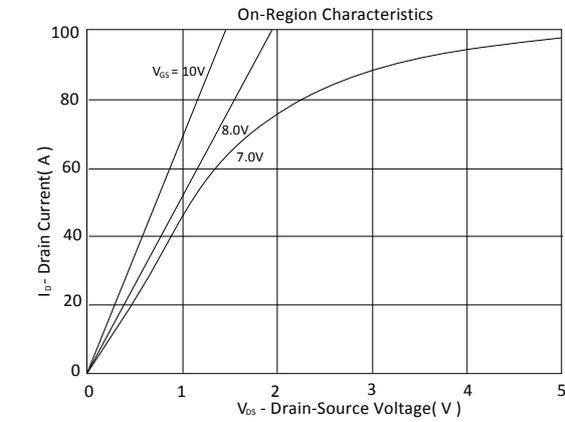
Ordering & Marking Information:

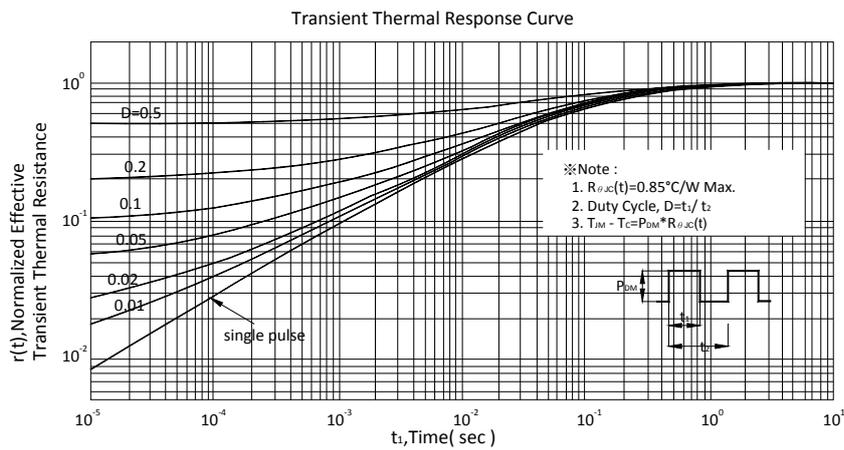
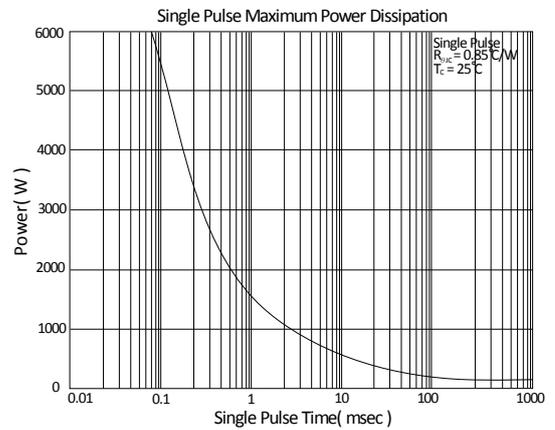
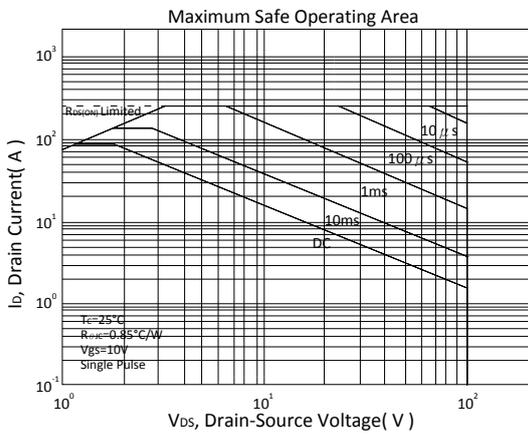
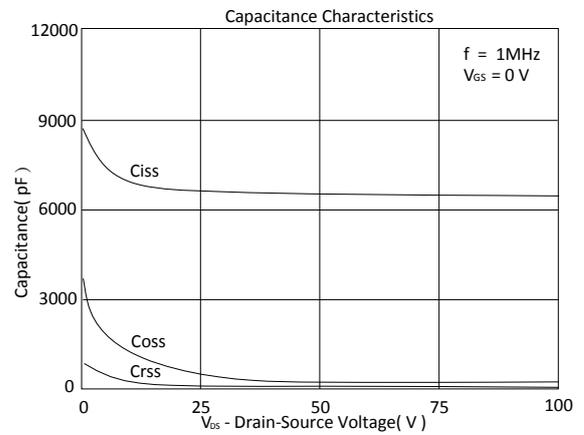
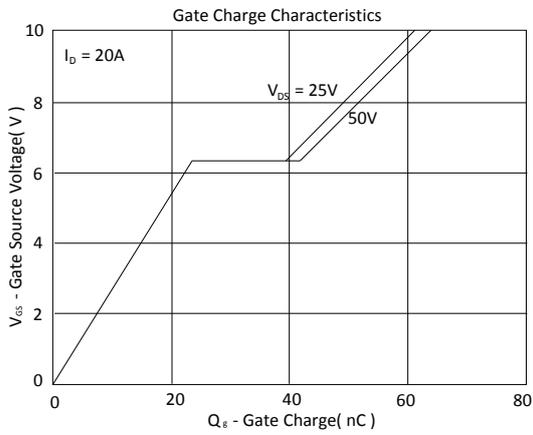
Device Name: EMD14N10E for TO-220





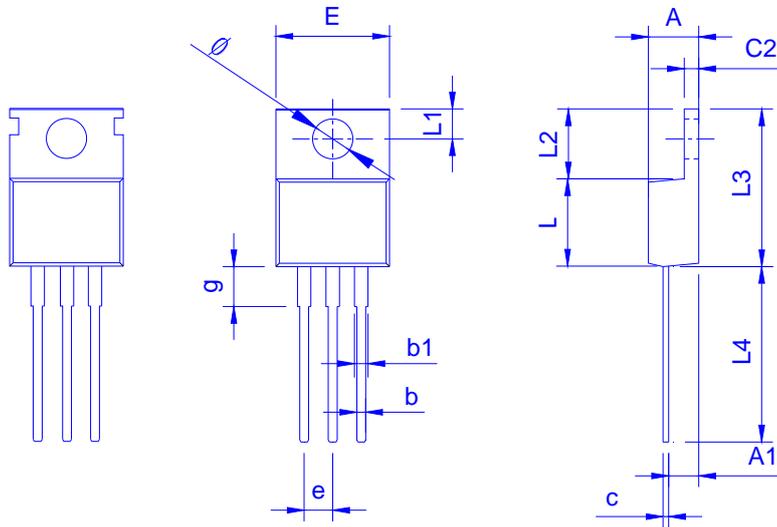
TYPICAL CHARACTERISTICS







Outline Drawing



Dimension in mm

Dimension	A	A1	b	b1	c	c2	E	L	L1	L2	L3	L4	φ	e	g
Min.	4.07	2.04	0.60	1.15	0.31	1.11	9.90	8.30	2.50	6.00	14.30	12.70	3.40	2.04	2.85
Typ.	4.44	2.40	0.80	1.27	-	1.27	10.16	-	2.74	6.30	15.00	13.40	3.84	2.54	3.71
Max.	4.82	3.00	1.00	1.75	0.65	1.41	11.50	9.75	3.25	6.80	16.90	14.50	4.00	3.04	4.10