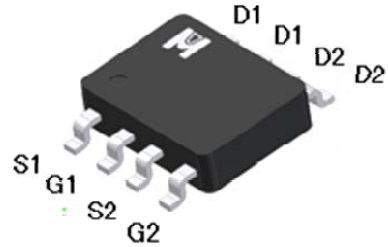
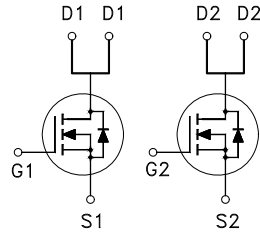


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	100V
$R_{DS(on)}$ (MAX.)	500m Ω
I_D	1.5A



UIS 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_A = 25^\circ\text{C}$	I_D	1.5	A
	$T_A = 100^\circ\text{C}$		0.9	
Pulsed Drain Current ¹		I_{DM}	6	
Power Dissipation	$T_A = 25^\circ\text{C}$	P_D	2	W
	$T_A = 100^\circ\text{C}$		0.8	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		25	$^\circ\text{C} / \text{W}$
Junction-to-Ambient ³	$R_{\theta JA}$		62.5	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$

³62.5 $^\circ\text{C} / \text{W}$ when mounted on a 1 in² pad of 2 oz copper.



ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	100			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1	2	3	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 80V, V _{GS} = 0V			1	μA
		V _{DS} = 70V, V _{GS} = 0V, T _J = 125 °C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 5V, V _{GS} = 10V	1.5			A
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = 10V, I _D = 1.5A		450	500	mΩ
		V _{GS} = 5V, I _D = 0.5A		485	570	
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 1.5A		2		S
DYNAMIC						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = 50V, f = 1MHz		328		pF
Output Capacitance	C _{oss}			35		
Reverse Transfer Capacitance	C _{rss}			21		
Total Gate Charge ^{1,2}	Q _g	V _{DS} = 15V, V _{GS} = 10V, I _D = 1.5A		7.6		nC
Gate-Source Charge ^{1,2}	Q _{gs}			1.1		
Gate-Drain Charge ^{1,2}	Q _{gd}			2.7		
Turn-On Delay Time ^{1,2}	t _{d(on)}	V _{DS} = 15V, I _D = 1A, V _{GS} = 10V, R _{GS} = 6Ω		12		nS
Rise Time ^{1,2}	t _r			15		
Turn-Off Delay Time ^{1,2}	t _{d(off)}			25		
Fall Time ^{1,2}	t _f			20		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I _S				1.5	A
Pulsed Current ³	I _{SM}				6	
Forward Voltage ¹	V _{SD}	I _F = I _S , V _{GS} = 0V			1.2	V
Reverse Recovery Time	t _{rr}			30		nS
Reverse Recovery Charge	Q _{rr}			60		nC

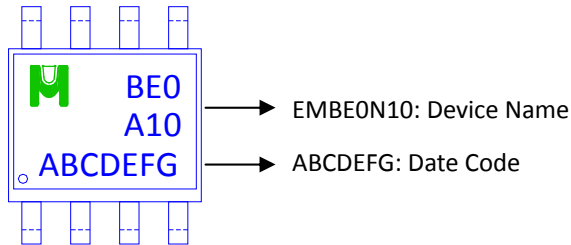
¹Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

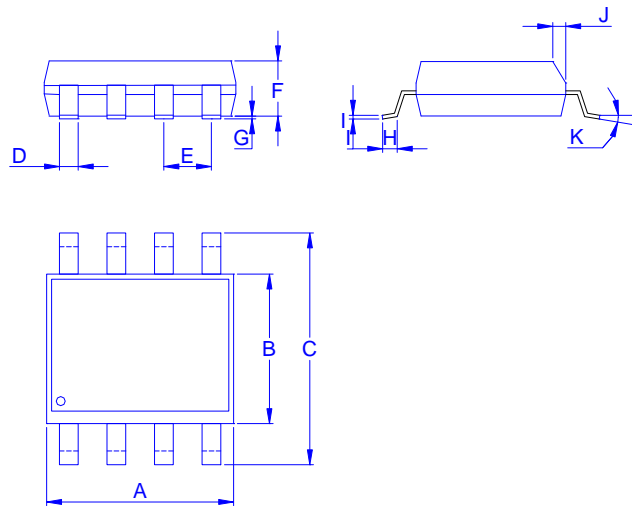
³Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: EMBE0A10G for SOP-8



Outline Drawing



Dimension in mm

Dimension	A	B	C	D	E	F	G	H	I	J	K
in.	4.70	3.70	5.80	0.33		1.20	0.08	0.40	0.19	0.25	0°
Typ.					1.27						
Max.	5.10	4.10	6.20	0.51		1.62	0.28	0.83	0.26	0.50	8°

