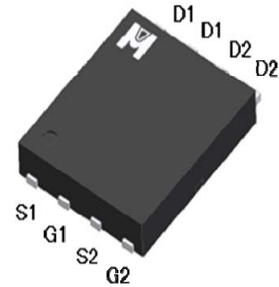
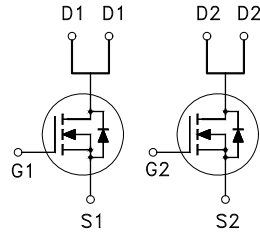


Dual N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	100V
$R_{DS(on)}$ (MAX.)	220m Ω
I_D	5.7A



UIS 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_C = 25\text{ }^\circ\text{C}$	I_D	5.7	A
	$T_C = 100\text{ }^\circ\text{C}$		3.6	
Pulsed Drain Current ¹		I_{DM}	22	
Avalanche Current		I_{AS}	3	
Avalanche Energy	$L = 0.1\text{mH}, I_D = 3\text{A}, R_G = 25\Omega$	E_{AS}	0.45	mJ
Repetitive Avalanche Energy ²	$L = 0.05\text{mH}$	E_{AR}	0.225	
Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	P_D	12.5	W
	$T_C = 100\text{ }^\circ\text{C}$		5	
Operating Junction & Storage Temperature Range		T_{j}, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		10	$^\circ\text{C} / \text{W}$
Junction-to-Ambient ³	$R_{\theta JA}$		75	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$

³75 $^\circ\text{C} / \text{W}$ when mounted on a 1 in² pad of 2 oz copper.



ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT		
			MIN	TYP	MAX			
STATIC								
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	100			V		
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1	1.5	2.9			
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA		
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 80V, V _{GS} = 0V			1	μA		
		V _{DS} = 70V, V _{GS} = 0V, T _J = 125 °C			25			
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 5V, V _{GS} = 10V	5.7			A		
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = 10V, I _D = 3A		185	220	mΩ		
		V _{GS} = 4.5V, I _D = 2A		215	260			
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 3A		4		S		
DYNAMIC								
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = 50V, f = 1MHz		858		pF		
Output Capacitance	C _{oss}			38				
Reverse Transfer Capacitance	C _{rss}			27				
Total Gate Charge ^{1,2}	Q _g (V _{GS} =10V)	V _{DS} = 15V, V _{GS} = 10V, I _D = 2A		14.3	20	nC		
	Q _g (V _{GS} =5V)			8	10			
Gate-Source Charge ^{1,2}	Q _{gs}			2.9				
Gate-Drain Charge ^{1,2}	Q _{gd}			3.4				
Turn-On Delay Time ^{1,2}	t _{d(on)}		V _{DS} = 15V, I _D = 1A, V _{GS} = 10V, R _{GS} = 6Ω		20			nS
Rise Time ^{1,2}	t _r				30			
Turn-Off Delay Time ^{1,2}	t _{d(off)}			36				
Fall Time ^{1,2}	t _f			30				
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)								
Continuous Current	I _S				5.7	A		
Pulsed Current ³	I _{SM}				22			
Forward Voltage ¹	V _{SD}	I _F = I _S , V _{GS} = 0V			1.2	V		
Reverse Recovery Time	t _{rr}			50		nS		
Reverse Recovery Charge	Q _{rr}			90		nC		

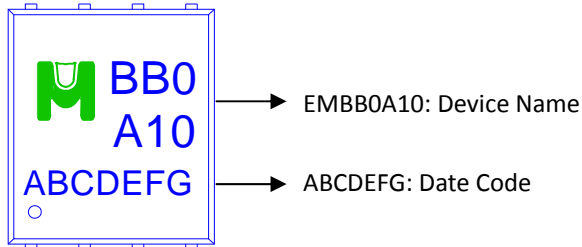
¹Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

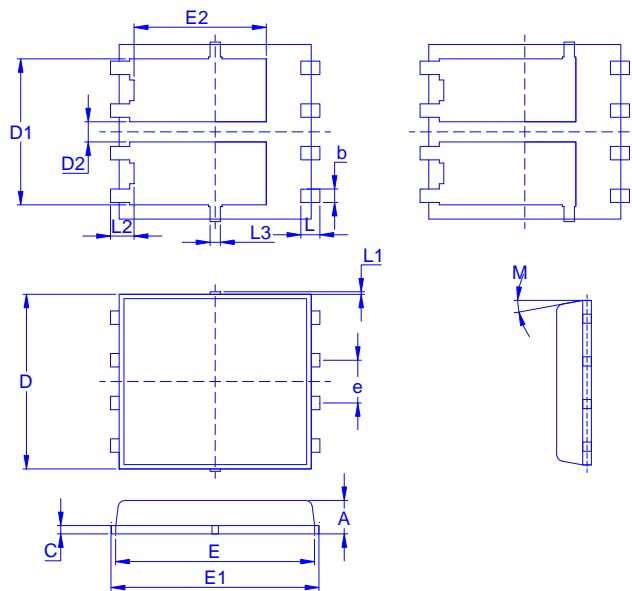
³Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: EMBB0A10H for EDFN 5 x 6



Outline Drawing



Dimension in mm

Dimension	A	b	c	D	D1	D2	E	E1	E2	e	L	L1	L2	M
Min.	0.85	0.3	0.15	4.8	3.41	0.47	5.65	5.95	3.30		0.38	0	0.38	0°
Typ.	1.01	0.4	0.2	5	4.01	0.67	5.75	6.05	3.43	1.27	0.55	0.09	0.48	
Max.	1.17	0.5	0.25	5.2	4.61	0.87	5.85	6.15	3.58		0.71	0.18	0.58	12°

Recommended minimum pads

