

N-Channel Logic Level Enhancement Mode Field Effect Transistor

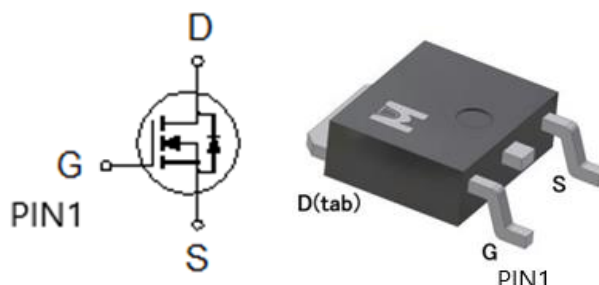
Product Summary:

	N-CH
BV_{DSS}	100V
$R_{DS(on)} (MAX.) @ V_{GS}=10V$	135m Ω
$R_{DS(on)} (MAX.) @ V_{GS}=4.5V$	170m Ω
$I_D @ T_C=25^{\circ}C$	10A

N Channel MOSFET

UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ($T_C = 25^{\circ}C$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_C = 25^{\circ}C$	I_D	10	A
	$T_C = 100^{\circ}C$		7	
Pulsed Drain Current ¹		I_{DM}	58	
Avalanche Current	$L = 0.01mH$	I_{AS}	5	mJ
Avalanche Energy	$L = 1.0mH$	E_{AS}	3.0	
Repetitive Avalanche Energy ²	$L = 0.5mH$	E_{AR}	1.5	
Power Dissipation	$T_C = 25^{\circ}C$	P_D	50	W
	$T_C = 100^{\circ}C$		20	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^{\circ}C$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		2.5	$^{\circ}C / W$
Junction-to-Ambient	$R_{\theta JA}$		75	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$

³75 $^{\circ}C / W$ when mounted on a 1 in² pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^{\circ}\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	100			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1.0	1.8	3.0	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 80V, V _{GS} = 0V			1	μA
		V _{DS} = 70V, V _{GS} = 0V, T _J = 125 °C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 10V, V _{GS} = 10V	10			A
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = 10V, I _D = 8A		115	135	mΩ
		V _{GS} = 4.5V, I _D = 5A		145	170	
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 8A		8		S
DYNAMIC						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = 25V, f = 1MHz		210		pF
Output Capacitance	C _{oss}			70		
Reverse Transfer Capacitance	C _{rss}			10		
Gate Resistance	R _g	V _{GS} = 15mV, V _{DS} = 0V, f = 1MHz		1.0		Ω
Total Gate Charge ^{1,2}	Q _g	V _{DS} = 80V, V _{GS} = 10V, I _D = 8A		6.4		nC
Gate-Source Charge ^{1,2}	Q _{gs}			0.6		
Gate-Drain Charge ^{1,2}	Q _{gd}			2.4		
Turn-On Delay Time ^{1,2}	t _{d(on)}	V _{dd} =50V, I _D =14A, R _g =6.8 ohm, V _{gs} =10V		4.6		nS
Rise Time ^{1,2}	t _r			4.3		
Turn-Off Delay Time ^{1,2}	t _{d(off)}			12.9		
Fall Time ^{1,2}	t _f			1.7		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T _c = 25 °C)						
Continuous Current	I _S				10	A
Pulsed Current ³	I _{SM}				58	
Forward Voltage ¹	V _{SD}	I _F = 1A, V _{GS} = 0V			1.3	V
Reverse Recovery Time	t _{rr}	I _F =14A, di/dt=100 A/uS		50.5		nS
Reverse Recovery Charge	Q _{rr}			35.7		nC

¹Pulse test : Pulse Width $\leq 300\text{ }\mu\text{sec}$, Duty Cycle $\leq 2\%$.

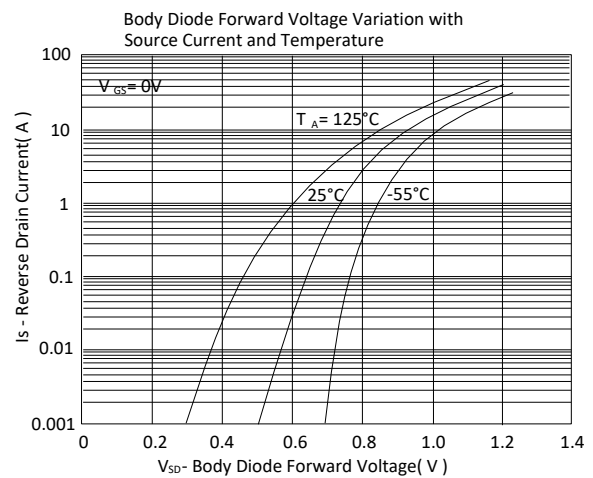
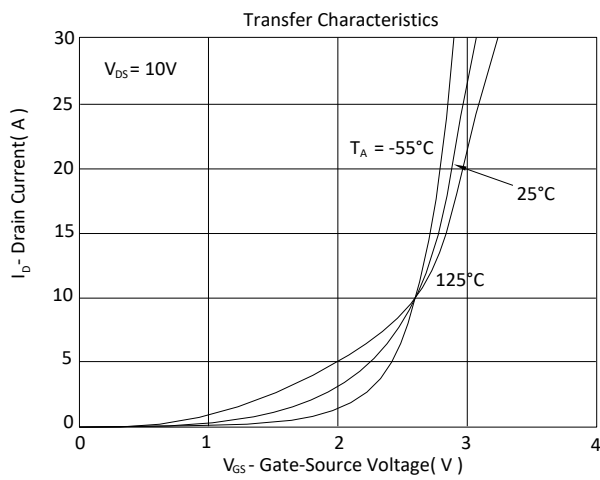
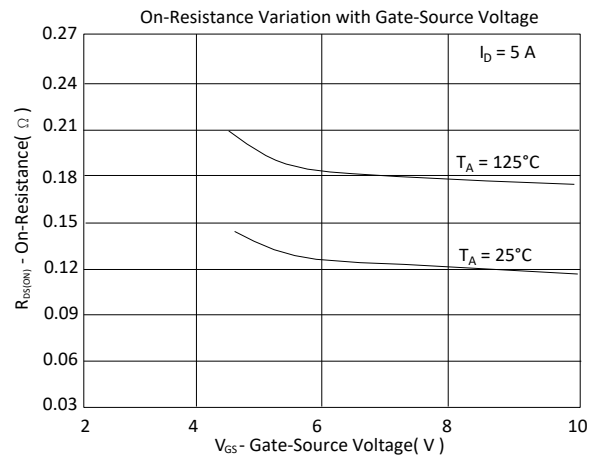
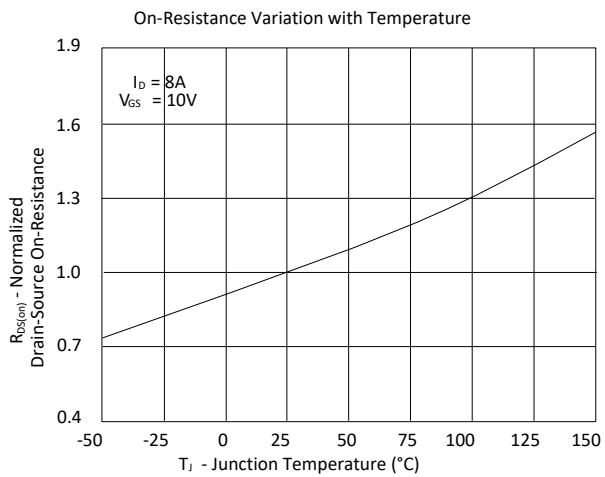
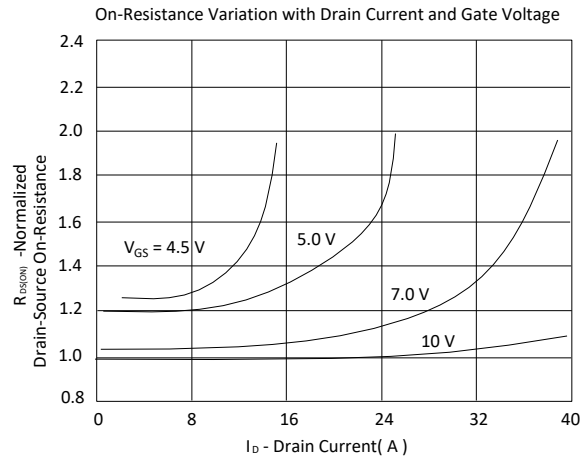
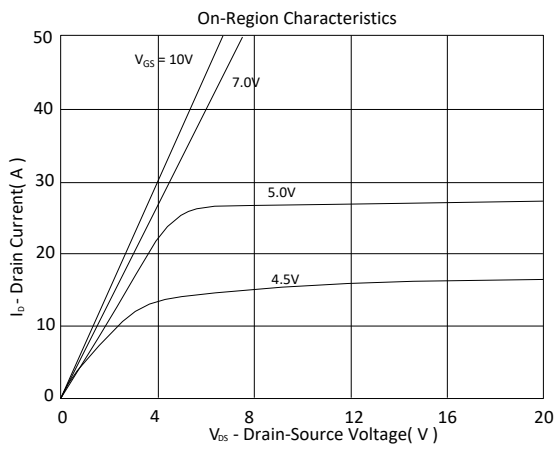
²Independent of operating temperature.

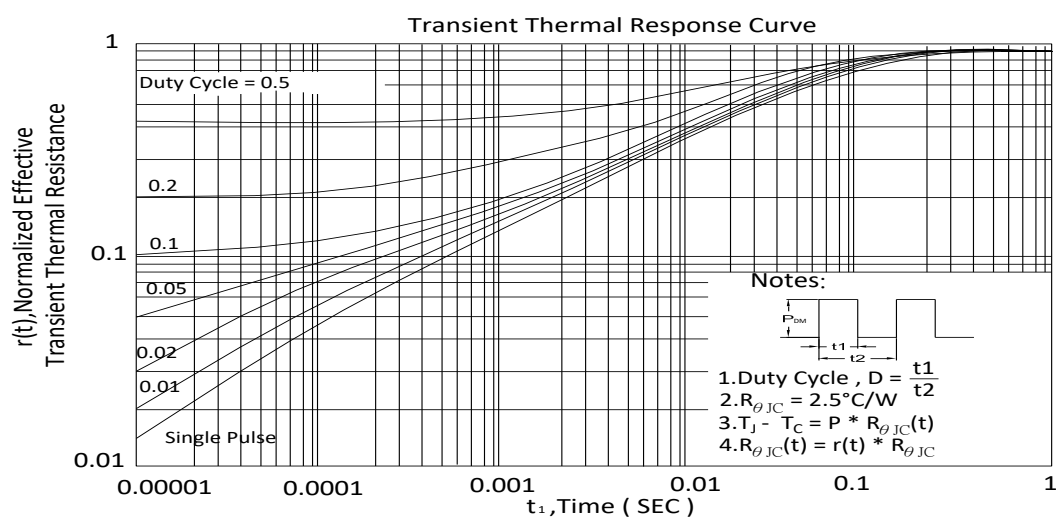
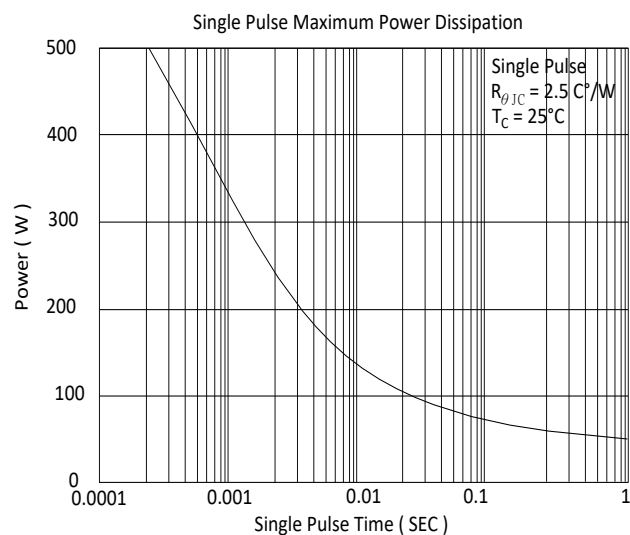
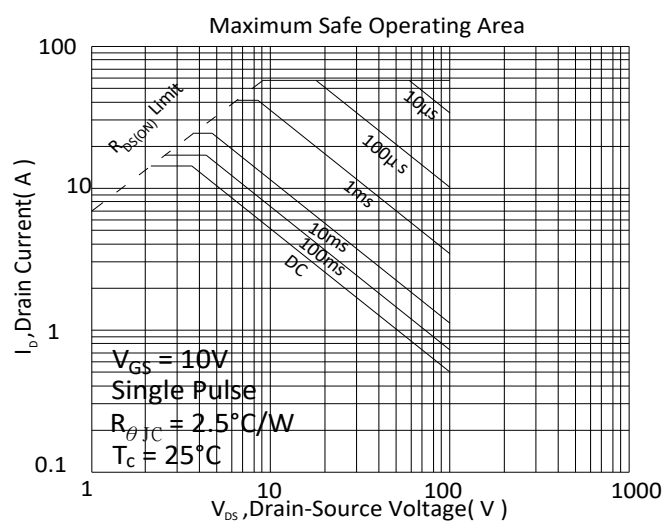
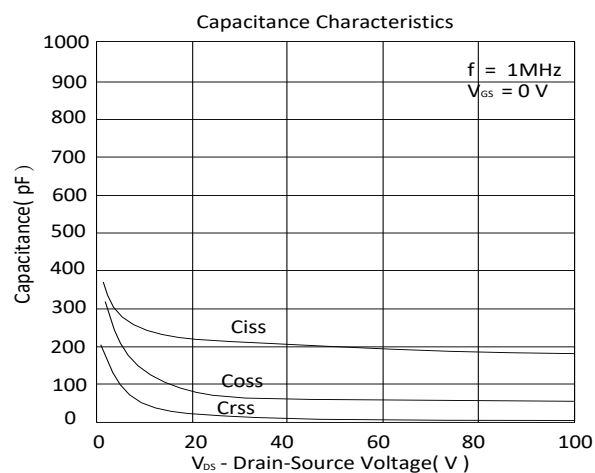
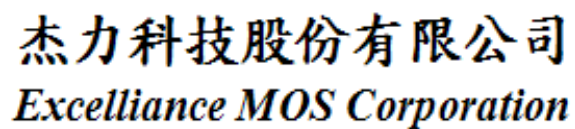
³Pulse width limited by maximum junction temperature.

EMC will review datasheet by quarter, and update new version.



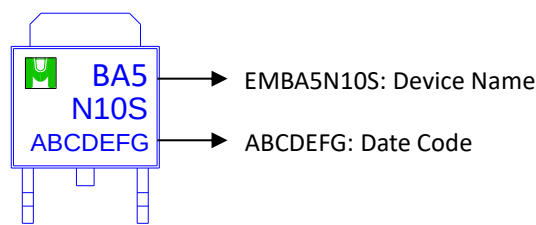
TYPICAL CHARACTERISTICS



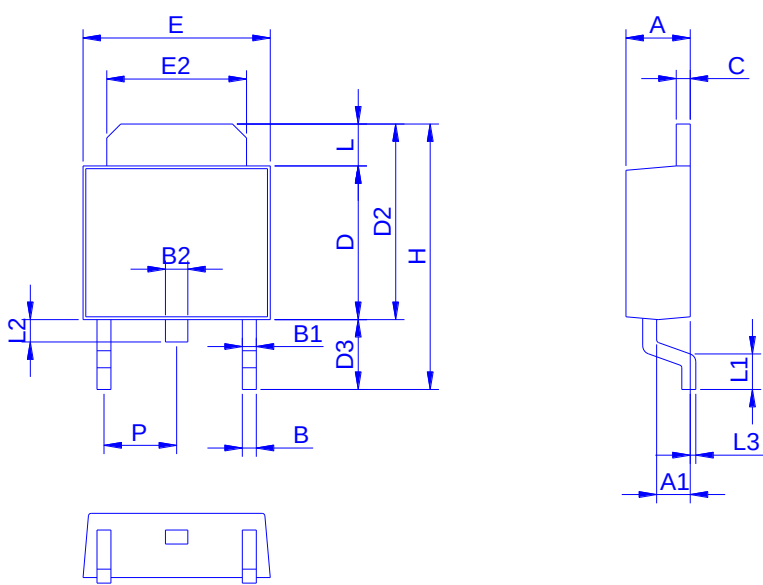


Ordering & Marking Information:

Device Name: EMBA5N10AS for DPAK (TO252-2)

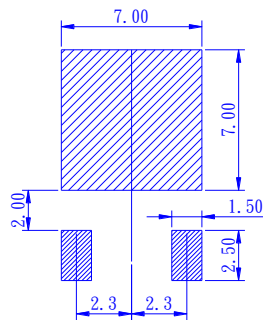


Outline Drawing

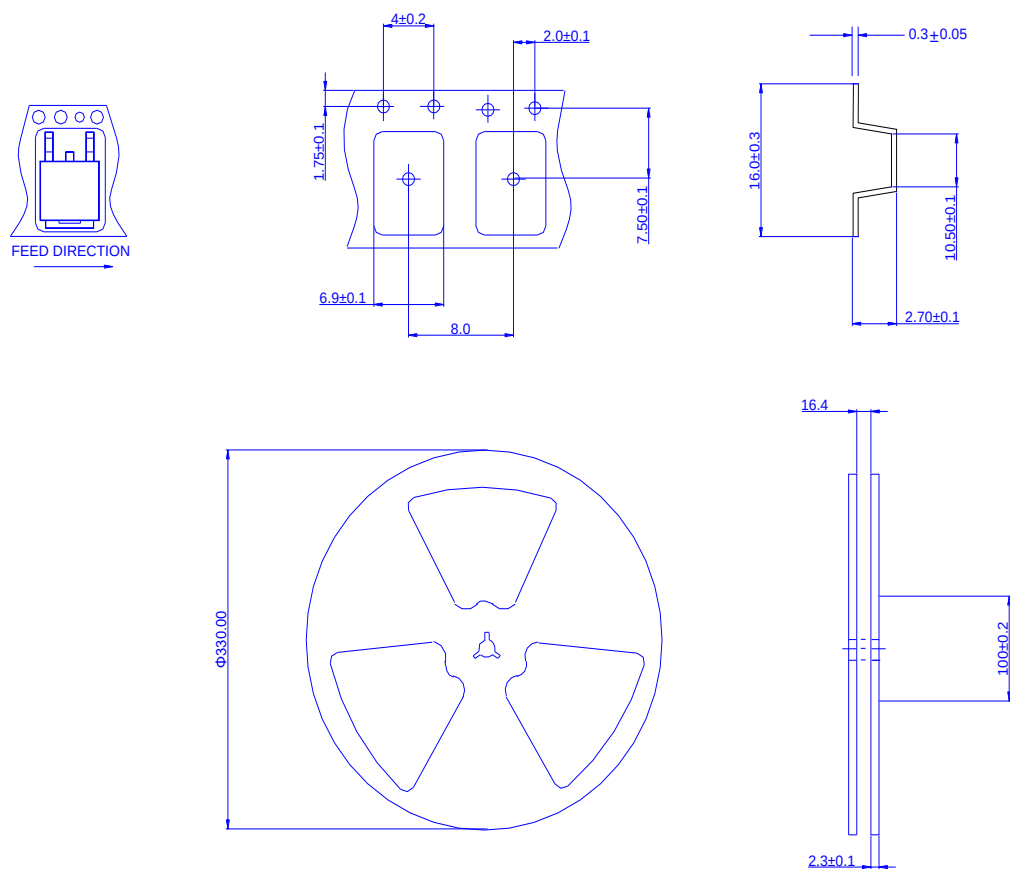


Dimension	A	A1	B	B1	B2	C	D	D2	D3	E	E2	H	L	L1	L2	L3	P
Min.	2.10	0.95	0.30	0.40	0.60	0.40	5.30	6.70	2.20	6.40	4.80	9.20	0.89	0.90	0.50	0.00	2.10
Max.	2.50	1.30	0.85	0.94	1.00	0.60	6.20	7.30	3.00	6.70	5.45	10.15	1.70	1.65	1.10	0.30	2.50

Footprint



◆ Tape&Reel Information:2500pcs/Reel(Dimension in millimeter)



產品別	TO252-2
Reel 尺寸	13"
編帶方式	FEED DIRECTION 
前空格	35
後空格	35
裝箱數	
滿捲數量	2.5K
捲/內盒比	1 : 1
內盒滿箱數	2.5K
內/外箱比	10 : 1