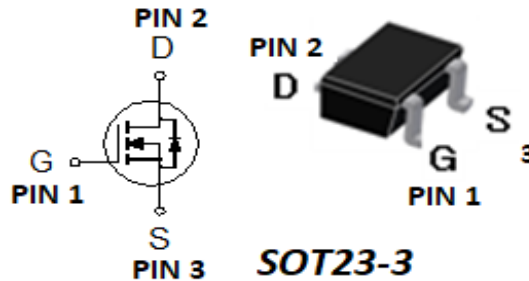


Single N-Channel Logic Level Enhancement Mode Field Effect Transistor

•Product Summary:

	N-CH
BVDSS	100V
$R_{DS(on)(MAX.)@V_{GS}=10V}$	100mΩ
$R_{DS(on)(MAX.)@V_{GS}=4.5V}$	150mΩ
$I_D @T_A=25^{\circ}C$	2A
$I_D @T_A=70^{\circ}C$	2A

• Pin Description:



Single N Channel MOSFET

UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free



•ABSOLUTE MAXIMUM RATINGS ($T_C = 25^{\circ}C$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNIT
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current	I_D	$T_A = 25^{\circ}C$	2
		$T_A = 70^{\circ}C$	2
Pulsed Drain Current ¹	I_{DM}	8	A
Avalanche Current	I_{AS}	2	
Avalanche Energy	L = 1mH	EAS	2
Repetitive Avalanche Energy ²	L = 0.5mH	EAR	1
Power Dissipation	P_D	$T_A = 25^{\circ}C$	1
		$T_A = 70^{\circ}C$	0.7
Operating Junction & Storage Temperature Range	T_{j}, T_{stg}	-55 to 150	$^{\circ}C$

¹ 100% UIS testing in condition of $V_D=30V, L=0.1mH, V_G=10V, I_L=0.6A$, Rated $V_{DS}=100V$ N-CH

•THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Ambient ³	$R_{\theta JA}$		120	$^{\circ}C/W$
	$R_{\theta JA}(t \leq 10s)$		80	

¹ Pulse width limited by maximum junction temperature.

² Duty cycle < 1%

³ $120^{\circ}C / W$ when mounted on a $1 in^2$ pad of 2 oz copper.

⁴ Guarantee by Engineering test

▪ ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage ⁴	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250uA	100			V
Gate Threshold Voltage ⁴	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250uA	1.2	1.9	2.5	
Gate-Body Leakage ⁴	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current ⁴	I _{DSS}	V _{DS} = 80V, V _{GS} = 0V			1	uA
		V _{DS} = 70V, V _{GS} = 0V, T _J = 125 °C			25	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = 10V, V _{GS} = 10V	2			A
Drain-Source On-State Resistance ^{1,4}	R _{DS(ON)}	V _{GS} = 10V, I _D = 8A		75	100	mΩ
		V _{GS} = 4.5V, I _D = 5A		100	150	
Forward Transconductance ¹	g _{fs}	V _{DS} = 5V, I _D = 8A		8		S
DYNAMIC						
Input Capacitance ⁵	C _{iss}	V _{GS} = 0V, V _{DS} = 25V, f = 1MHz		221		pF
Output Capacitance ⁵	C _{oss}			93		
Reverse Transfer Capacitance ⁵	C _{rss}			28		
Gate Resistance ^{4,5}	R _g	f = 1MHz		1.0		Ω
Total Gate Charge ^{1,2,5}	Q _g (V _{GS} =10V)	V _{DS} = 80V, V _{GS} = 10V, I _D = 8A		6.5		nC
Gate-Source Charge ^{1,2,5}	Q _{gs}			1.3		
Gate-Drain Charge ^{1,2,5}	Q _{gd}			2.2		
Turn-On Delay Time ^{1,2,5}	t _{d(on)}	V _{DS} = 50V, V _{GS} = 10V, I _D = 5A, R _g = 3Ω		4.6		nS
Rise Time ^{1,2,5}	t _r			6.8		
Turn-Off Delay Time ^{1,2,5}	t _{d(off)}			10		
Fall Time ^{1,2,5}	t _f			8.6		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I _S				2	A
Pulsed Current ³	I _{SM}				8	
Forward Voltage ^{1,4}	V _{SD}	I _F = 1A, V _{GS} = 0V			1.3	V
Reverse Recovery Time ⁵	t _{rr}	I _F = 18A, dI _F /dt = 100A / uS		22		nS
Peak Reverse Recovery Current ⁵	I _{RM(REC)}			1.1		A
Reverse Recovery Charge ⁵	Q _{rr}			13		nC

¹Pulse test : Pulse Width ≤ 300 usec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

⁴Guarantee by FT test Item

⁵Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.

▪ TYPICAL CHARACTERISTICS

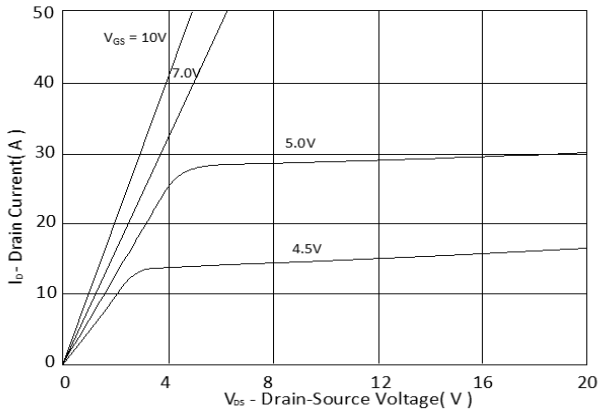


Fig.1 Typical Output Characteristics

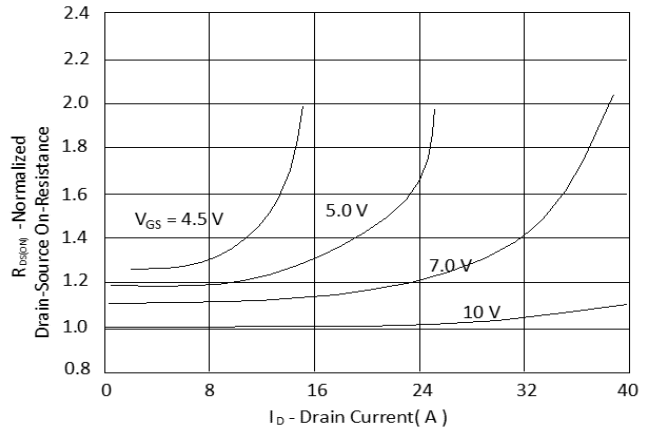


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

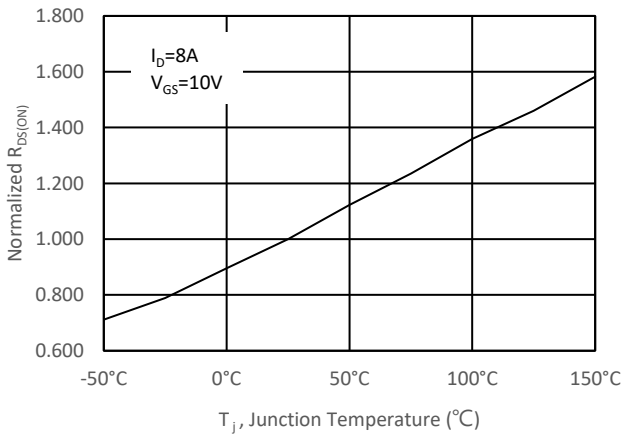


Fig.3 Normalized On-Resistance v.s. Junction Temperature

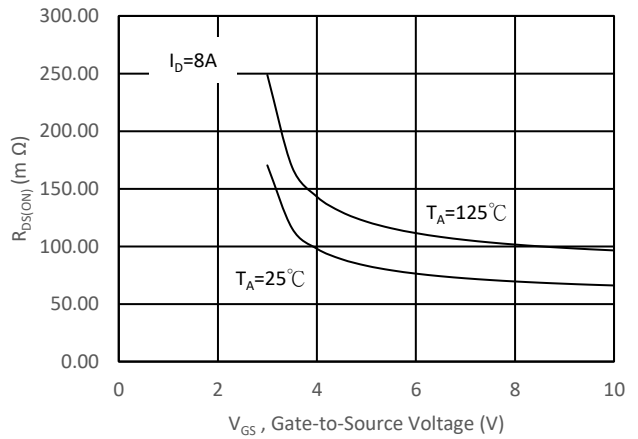


Fig.4 On-Resistance v.s. Gate Voltage

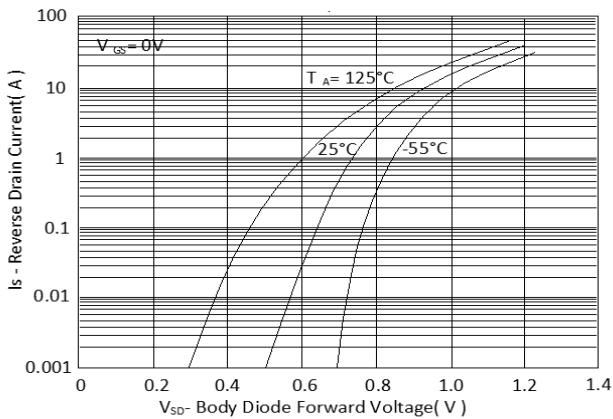


Fig.5 Forward Characteristic of Reverse Diode

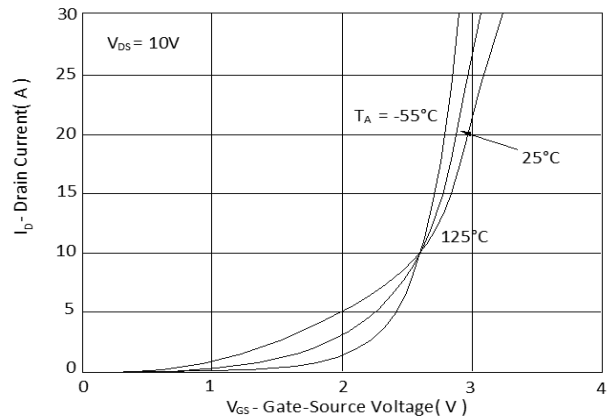


Fig.6 Transfer Characteristics

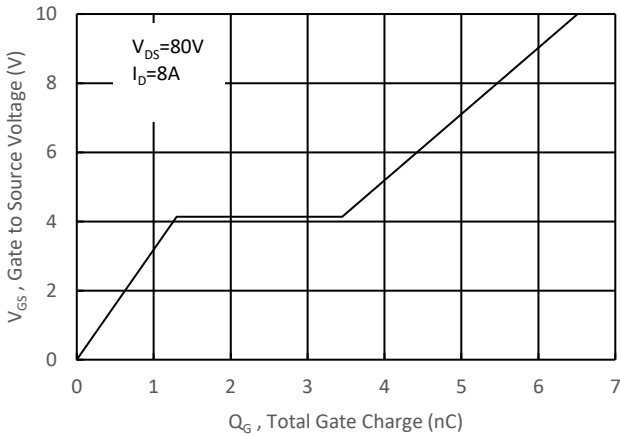


Fig.7 Gate Charge Characteristics

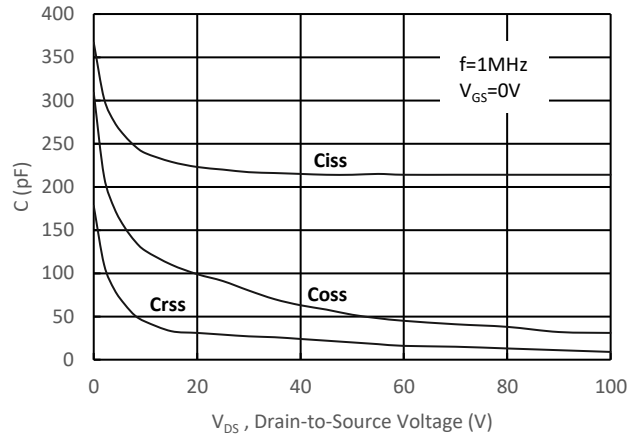


Fig.8 Typical Capacitance Characteristics

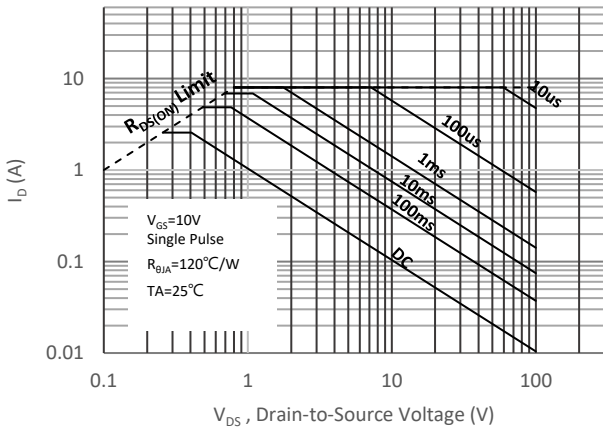


Fig 9. Maximum Safe Operating Area

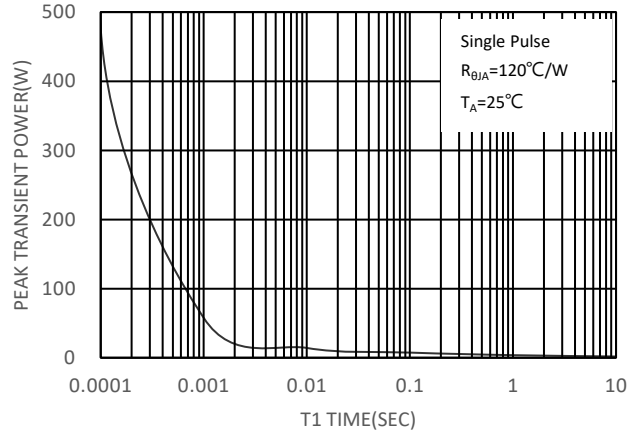


Fig 10. Single Pulse Maximum Power Dissipation

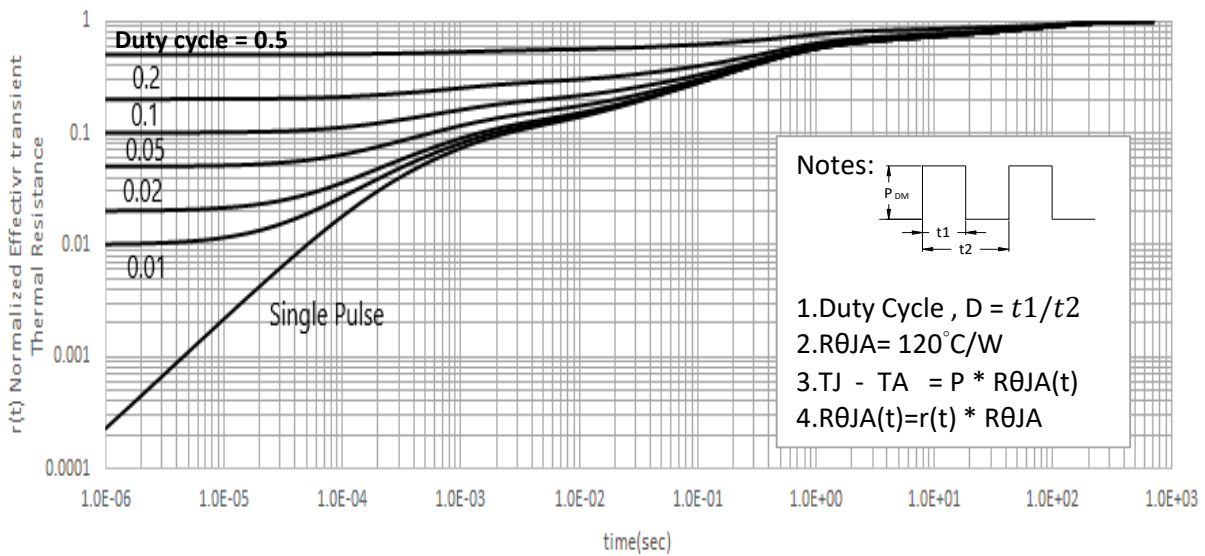
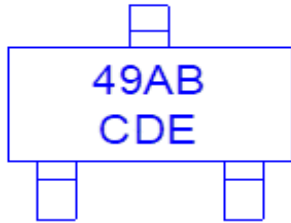


Fig 11. Effective Transient Thermal Impedance



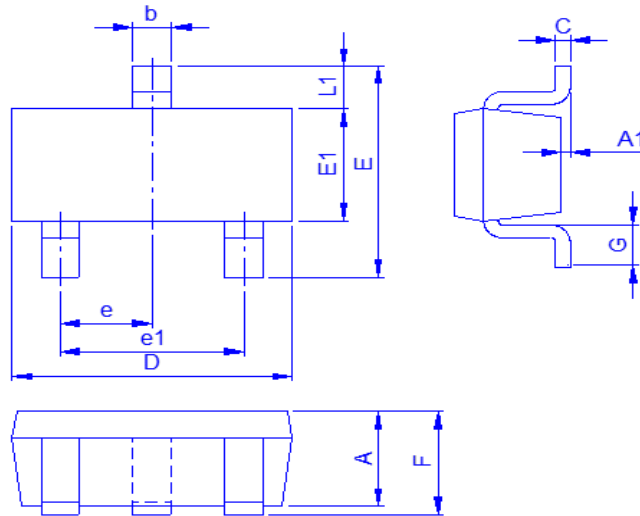
Ordering & Marking Information:

Device Name: EMBA2N10JSS for SOT-23-3



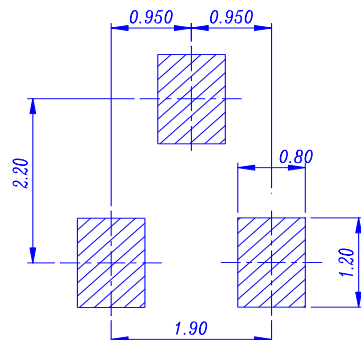
49 : Device Code, 49 for EMBA2N10JSS
A: Year(A:2008 B:2009 C:2010....)
B: Month(A:01 B:02 C:03 D:04 E:05 F:06
G:07 H:08 I:09 J:10 K:11 L:12)
CDE: Serial No.

Outline Drawing

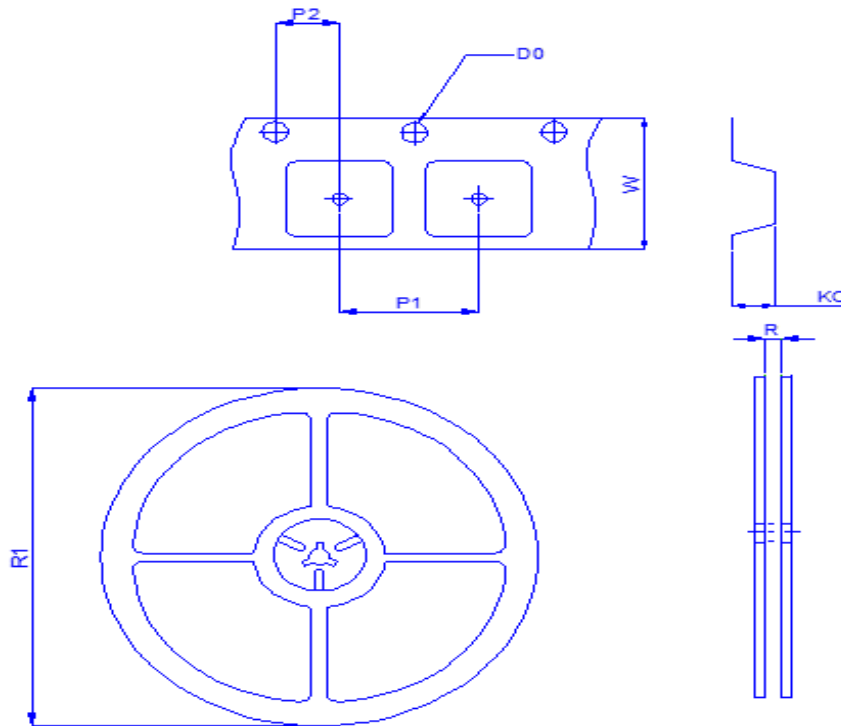


	A	A1	b	C	D	E	E1	e	e1	F	G	L1
Min.	0.88	0	0.3	0.08	2.8	2.1	1.2	0.9	1.8	0.89	0.3	0
Typ.	0.95	0	0	0	2.9	2.5	1.3	0.95	1.9	0	0	0.54
Max.	1.1	0.1	0.5	0.202	3.04	2.64	1.4	1	2	1.2	0.6	0

Footprint



◆ Tape&Reel Information:3000pcs/Reel (Dimension in millimeter)



產品別	SOT23-3
Reel尺寸	7"
編帶方式	<p>FEEED DIRECTION</p>

Dimension in mm

Dimension	Carrier tape					Reel	
	D0	K0	P1	P2	W	R	R1
Typ.	1.53	1.45	4	2	8	8.5	178
±	0.2	0.5	0.2	0.2	0.5	REF	REF