杰力科技股份有限公司
Excelliance MOS Corporation

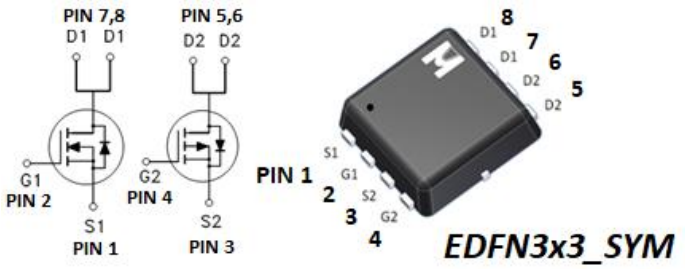
EMB60C06V

N-Channel + P-Channel Logic Level Enhancement Mode Field Effect Transistor

▪Product Summary:

	N-CH	P-CH
BVDSS	60V	-60V
$R_{DSON\ (MAX.)}$@V_{GS}=10V	60.0mΩ	90.0mΩ
$R_{DSON\ (MAX.)}$@V_{GS}=4.5V	85.0mΩ	135.0mΩ
I_D @T_C=25°C	13.0A	-10.0A
I_D @T_A=25°C	4.0A	-4.0A

▪ Pin Description:



N + P Channel MOSFET
UIS, Rg 100% Tested
Pb-Free Lead Plating & Halogen Free

▪ ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS		UNIT
			N-CH	P-CH	
Gate-Source Voltage		V_{GS}	±20	±20	V
Continuous Drain Current	T_C = 25 °C	I_D	13	-10	A
	T_C = 100 °C		8	-6	
Continuous Drain Current	T_A = 25 °C	I_D	4	-4	
	T_A = 70 °C		3	-3	
Pulsed Drain Current[1]		I_{DM}	52	-40	
Avalanche Current		I_{AS}	25	-26	
Avalanche Energy	L = 0.1mH	EAS	31.3	33.8	mJ
Repetitive Avalanche Energy[2]	L = 0.05mH	EAR	15.6	16.9	
Power Dissipation	T_C = 25 °C	P_D	16.7	16.7	W
	T_C = 100 °C		6.7	6.7	
Power Dissipation	T_A = 25 °C	P_D	2.3	2.3	W
	T_A = 70 °C		1.5	1.5	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150		°C

▪ 100% UIS testing in condition of VD=30V, L=0.1mH, VG=10V, IL=15A, Rated VDS=60V N-CH

▪ 100% UIS testing in condition of VD=30V, L=0.1mH, VG=10V, IL=16A, Rated VDS=-60V P-CH

▪THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM		UNIT
			N-CH	P-CH	
Junction-to-Case	$R_{\theta JC}$		7.5	7.5	°C/W
Junction-to-Ambient[3]	$R_{\theta JA}$		55	55	

[1]Pulse width limited by maximum junction temperature.

[2]Duty cycle < 1%

[3]55°C / W when mounted on a 1 in^2 pad of 2 oz copper.

[4]Guarantee by Engineering test

▪ **N-CH_ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)**

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage[4]	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250uA	60			V
Gate Threshold Voltage[4]	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250uA	1	1.6	3	
Gate-Body Leakage[4]	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current[4]	I_{DSS}	V_{DS} = 48V, V_{GS} = 0V			1	uA
		V_{DS} =42V, V_{GS} =0V, T_J = 125 °C			25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10V, V_{GS} = 10V	13			A
Drain-Source On-State Resistance[1,4]	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 10A		50	60	mΩ
		V_{GS} = 4.5V, I_D = 8A		60	85	
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 10A		13		S
DYNAMIC						
Input Capacitance[5]	C_{iss}	V_{GS} = 0V, V_{DS} = 30V, f = 1MHz		602		pF
Output Capacitance[5]	C_{oss}			72		
Reverse Transfer Capacitance[5]	C_{rss}			40		
Gate Resistance[4,5]	R_g	f = 1MHz		1.3		Ω
Total Gate Charge[1,2,5]	Q_g(V_{GS}=10V)	V_{DS} = 30V, V_{GS} = 10V, I_D = 10A		15.3		nC
	Q_g(V_{GS}=4.5V)			8.0		
Gate-Source Charge[1,2,5]	Q_{gs}			2.1		
Gate-Drain Charge[1,2,5]	Q_{gd}			4.9		
Turn-On Delay Time[1,2,5]	$t_{d(on)}$	V_{DS} = 30V, V_{GS} = 10V, I_D = 5A , Rg = 6Ω		5.7		nS
Rise Time[1,2,5]	t_r			6.7		
Turn-Off Delay Time[1,2,5]	$t_{d(off)}$			14.2		
Fall Time[1,2,5]	t_f			1.8		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				13	A
Pulsed Current[3]	I_{SM}				52	
Forward Voltage[1,4]	V_{SD}	I_F = I_S, V_{GS} = 0V			1.3	V
Reverse Recovery Time[5]	t_{rr}	I_F = I_S, dI_F/dt = 100A / uS		19.2		nS
Peak Reverse Recovery Current[5]	$I_{RM(REC)}$			2.16		A
Reverse Recovery Charge[5]	Q_{rr}			18.7		nC

[1]Pulse test : Pulse Width ≦ 300 usec, Duty Cycle ≦ 2%.

[2]Independent of operating temperature.

[3]Pulse width limited by maximum junction temperature.

[4]Guarantee by FT test Item

[5]Guarantee by Engineering test

EMC will review datasheet by quarter, and update new version.

▪ N-CH_TYPICAL CHARACTERISTICS

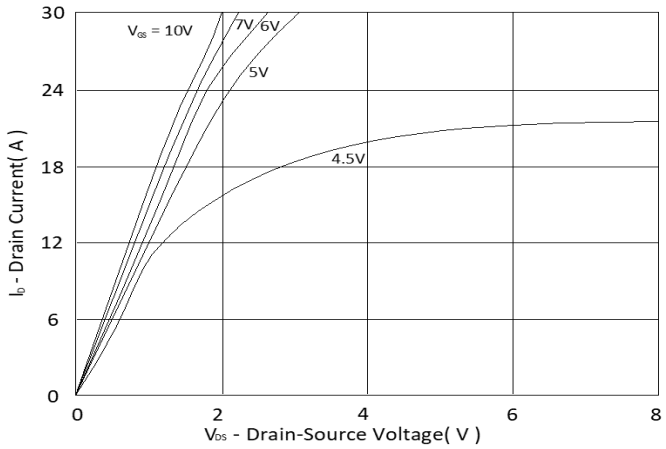


Fig.1 Typical Output Characteristics

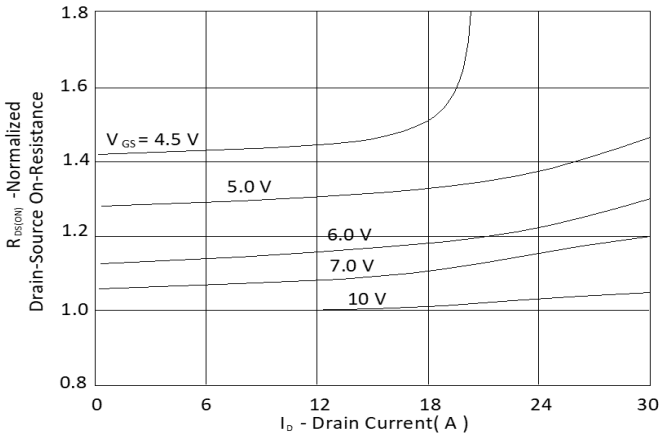


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

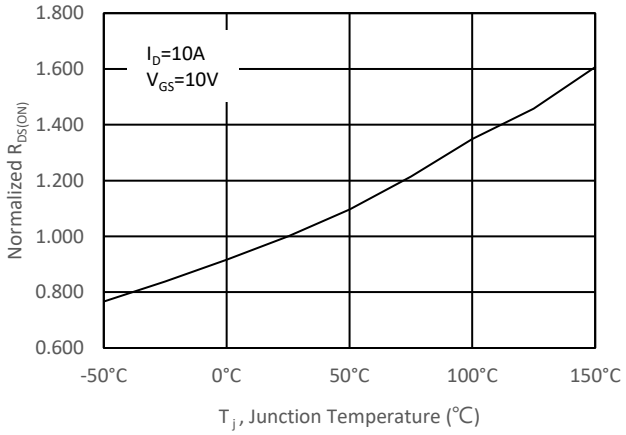


Fig.3 Normalized On-Resistance v.s. Junction Temperature

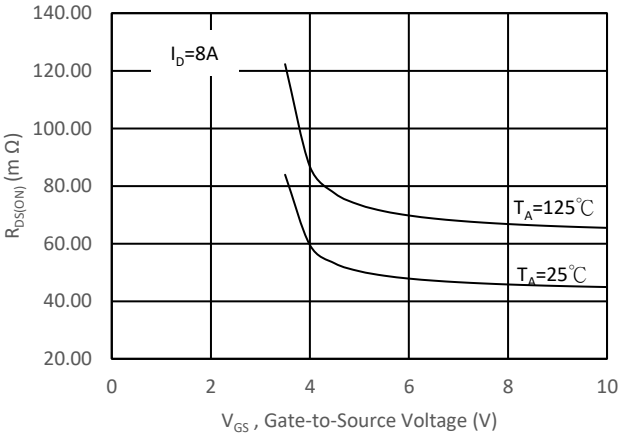


Fig.4 On-Resistance v.s. Gate Voltage

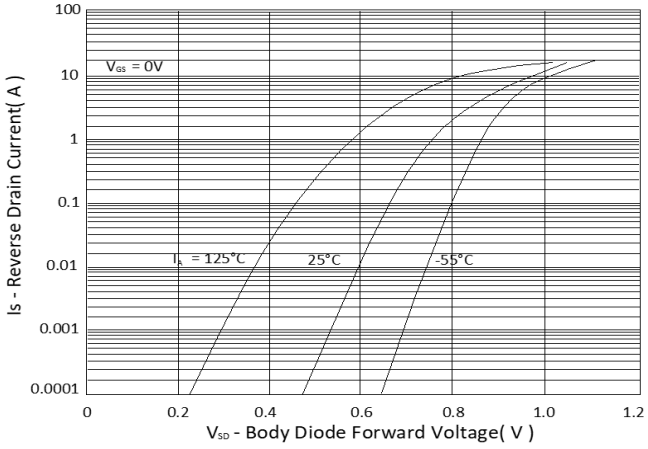


Fig.5 Forward Characteristic of Reverse Diode

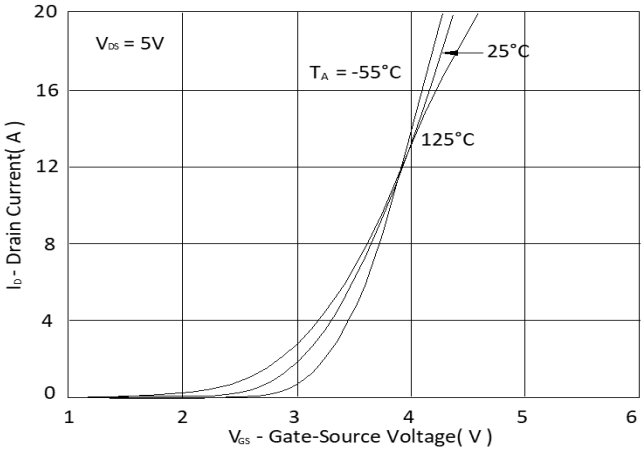


Fig.6 Transfer Characteristics

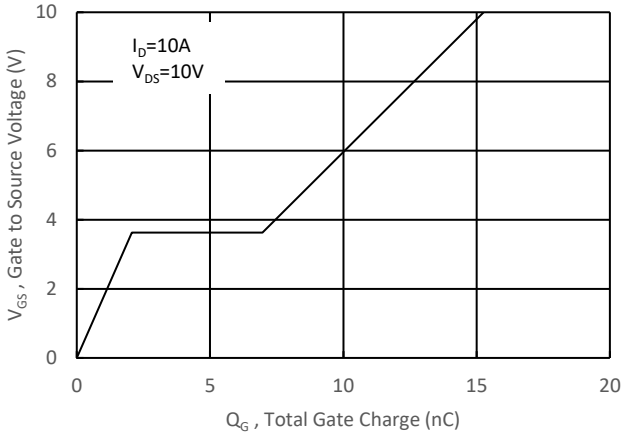


Fig.7 Gate Charge Characteristics

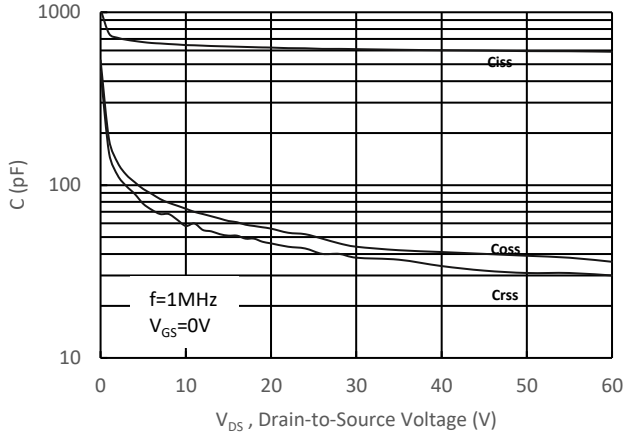


Fig.8 Typical Capacitance Characteristics

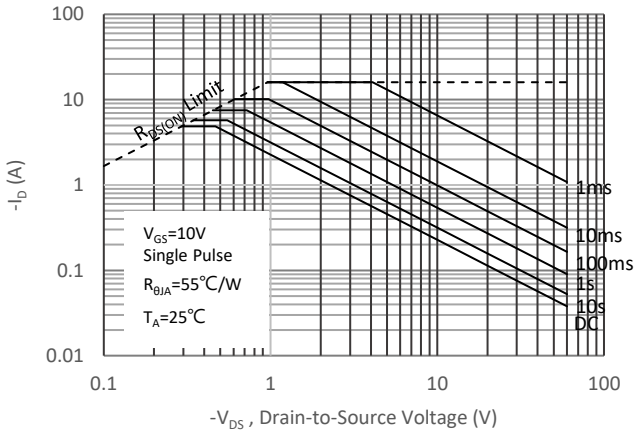


Fig 9. Maximum Safe Operating Area

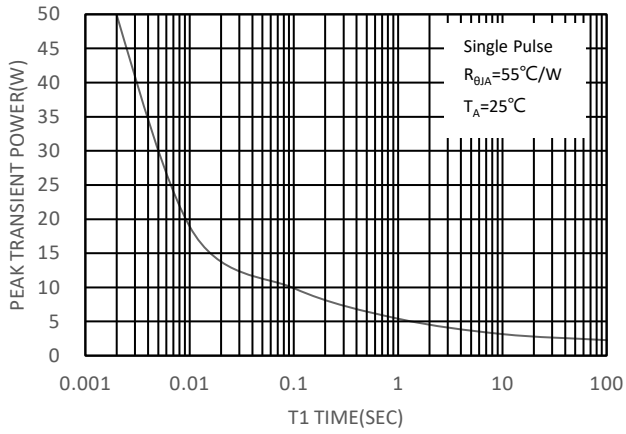


Fig 10. Single Pulse Maximum Power Dissipation

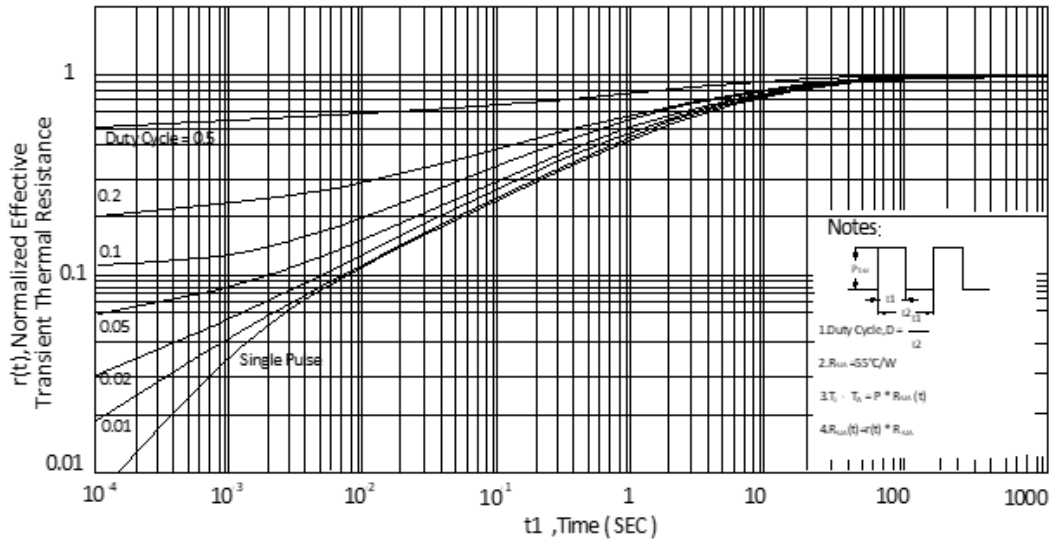


Fig 11. Effective Transient Thermal Impedance

▪ **P-CH_ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)**

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage[4]	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250uA	-60			V
Gate Threshold Voltage[4]	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250uA	-1	-1.6	-3	
Gate-Body Leakage[4]	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current[4]	I_{DSS}	V_{DS} = -48V, V_{GS} = 0V			1	uA
		V_{DS} =-42V, V_{GS} =0V, T_J = 125 °C			25	
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = 10V, V_{GS} = 10V	-10			A
Drain-Source On-State Resistance[1,4]	$R_{DS(ON)}$	V_{GS} = 10V, I_D = 8A		78	90	mΩ
		V_{GS} = 4.5V, I_D = 6A		100	135	
Forward Transconductance[1]	g_{fs}	V_{DS} = 5V, I_D = 8A		9		S
DYNAMIC						
Input Capacitance[5]	C_{iss}	V_{GS} = 0V, V_{DS} = -30V, f = 1MHz		945		pF
Output Capacitance[5]	C_{oss}			67		
Reverse Transfer Capacitance[5]	C_{rss}			56		
Gate Resistance[4,5]	R_g	f = 1MHz		5.1		Ω
Total Gate Charge[1,2,5]	Q_g(V_{GS}=10V)	V_{DS} = -30V, V_{GS} = -10V, I_D = -8A		20.2		nC
	Q_g(V_{GS}=4.5V)			10.5		
Gate-Source Charge[1,2,5]	Q_{gs}			2.1		
Gate-Drain Charge[1,2,5]	Q_{gd}			4.9		
Turn-On Delay Time[1,2,5]	$t_{d(on)}$	V_{DS} = -30V, V_{GS} = -10V, I_D = -5A , Rg = 6Ω		6.2		nS
Rise Time[1,2,5]	t_r			8.2		
Turn-Off Delay Time[1,2,5]	$t_{d(off)}$			45.4		
Fall Time[1,2,5]	t_f			29.0		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S				-10	A
Pulsed Current[3]	I_{SM}				-40	
Forward Voltage[1,4]	V_{SD}	I_F = I_S, V_{GS} = 0V			-1.3	V
Reverse Recovery Time[5]	t_{rr}	I_F = I_S, dI_F/dt = 100A / uS		19.5		nS
Peak Reverse Recovery Current[5]	$I_{RM(REC)}$			2.47		A
Reverse Recovery Charge[5]	Q_{rr}			19.0		nC

[1]Pulse test : Pulse Width ≦ 300 usec, Duty Cycle ≦ 2%.

[2]Independent of operating temperature.

[3]Pulse width limited by maximum junction temperature.

[4]Guarantee by FT test Item

[5]Guarantee by Engineering test

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▪ P-CH_TYPICAL CHARACTERISTICS

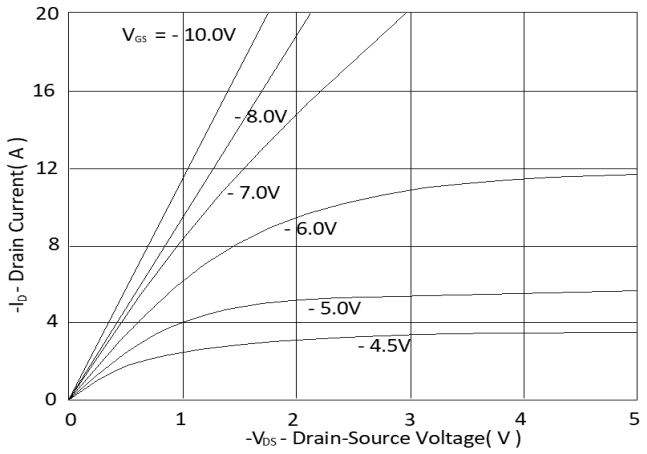


Fig.1 Typical Output Characteristics

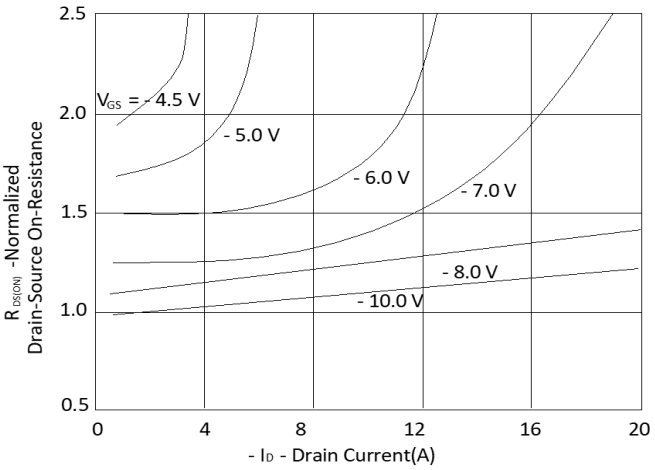


Fig.2 On-Resistance Variation with Drain Current and Gate Voltage

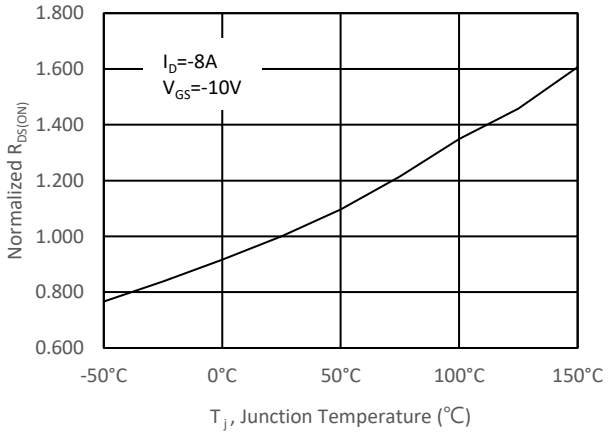


Fig.3 Normalized On-Resistance v.s. Junction Temperature

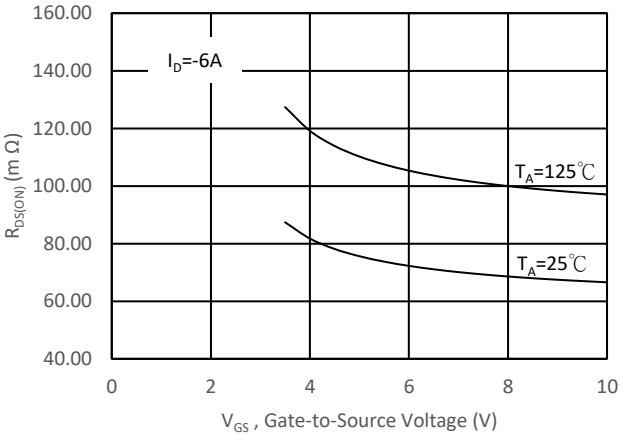


Fig.4 On-Resistance v.s. Gate Voltage

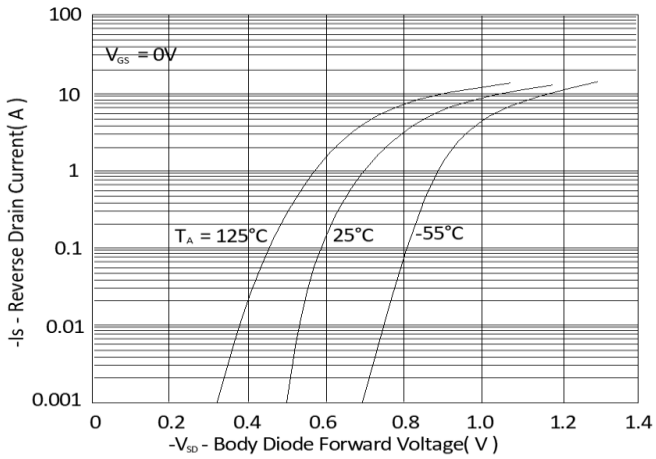


Fig.5 Forward Characteristic of Reverse Diode

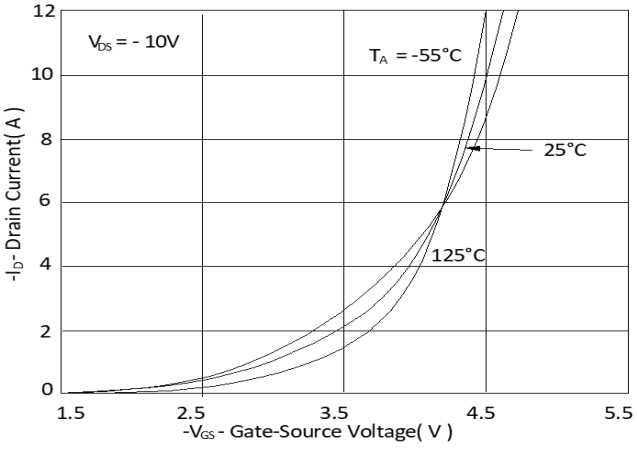


Fig.6 Transfer Characteristics

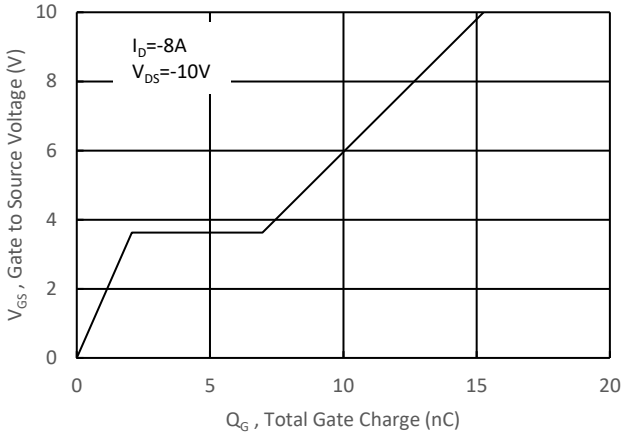


Fig.7 Gate Charge Characteristics

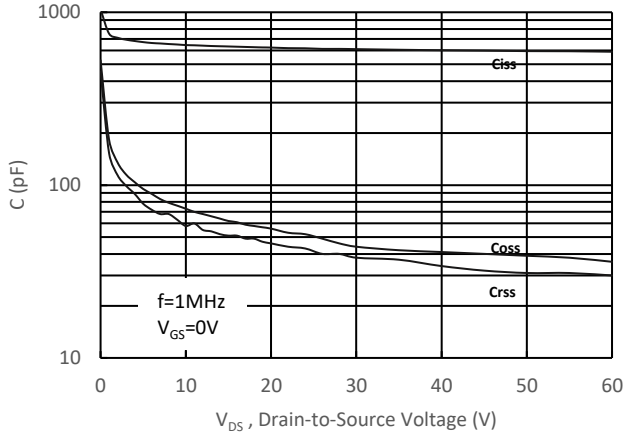
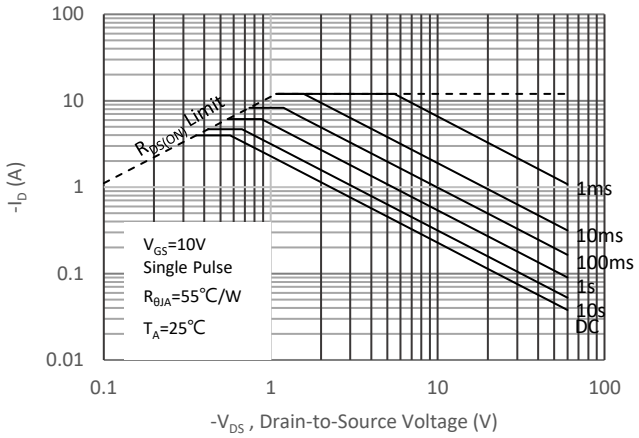


Fig.8 Typical Capacitance Characteristics



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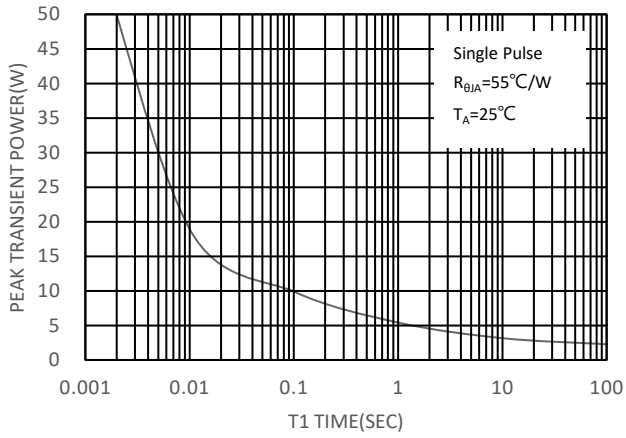

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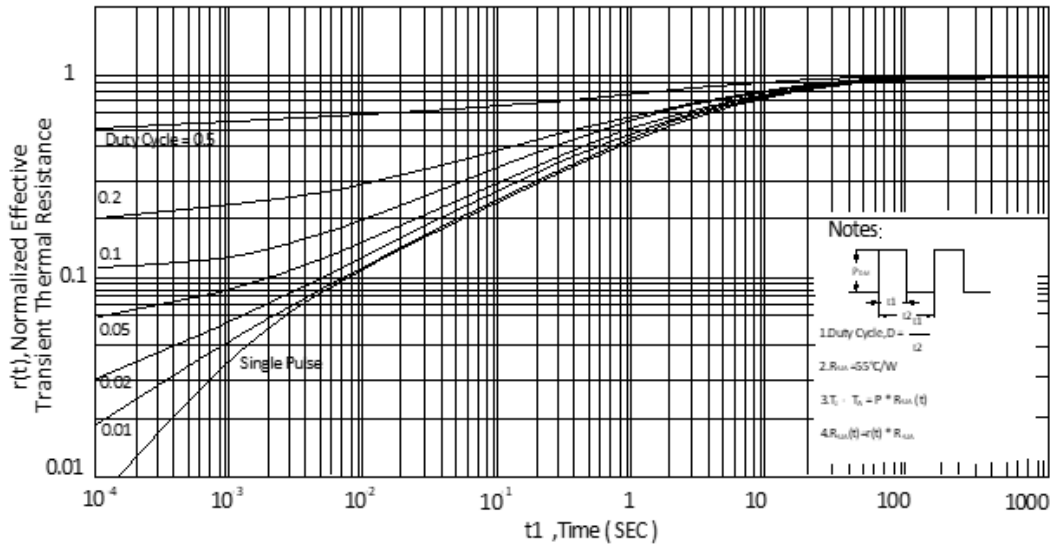


Fig 11. Effective Transient Thermal Impedance

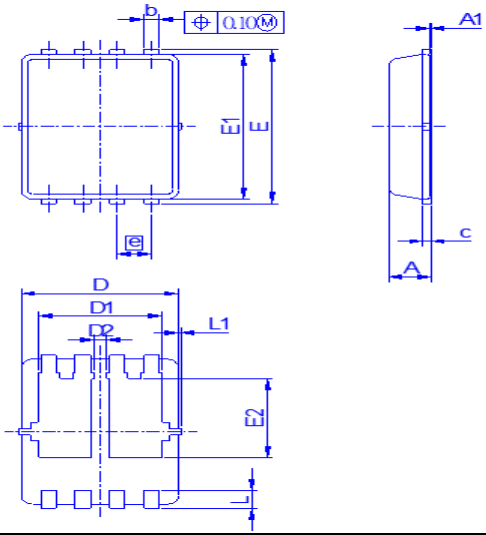
Ordering & Marking Information:

Device Name: EMB60C06V for EDFN 3x3

B60C06: Device Name

ABCDEFG: Date Code
A: Assembly House
B: Year(A:2008 B:2009 C:2010….)
C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)
DEFG: Serial No

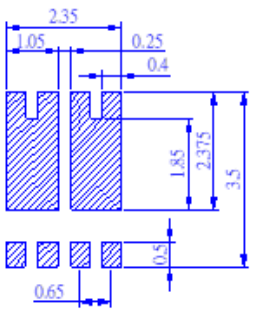
Outline Drawing



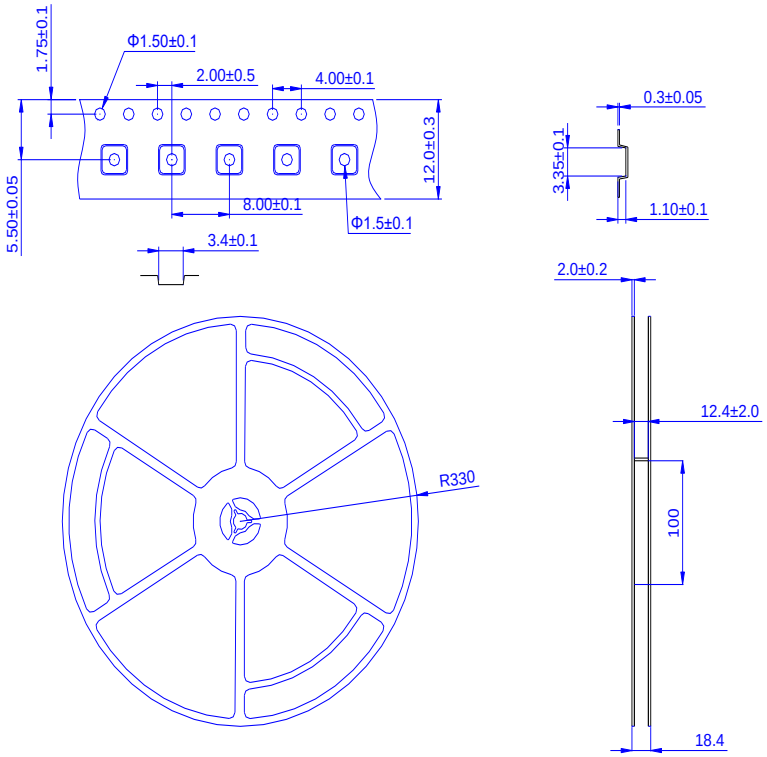
Dimension	A	A1	b	c	D	D1	D2	E	E1	E2	e	L
Min.	0.65	0	0.2	0.1	2.9	2.15	0.28	3.1	2.9	1.53	0.55	0.3
Typ.	0.75	-	0.3	0.15	3	2.47	0.38	3.2	3	1.81	0.65	0.4
Max.	0.9	0.05	0.4	0.25	3.3	2.75	-	3.5	3.3	1.98	0.75	0.5

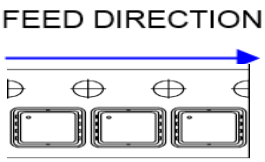
Dimension	L1	θ1
Min.	-	0°
Typ.	0.075	10°
Max.	0.15	14°

Footprint



◆ **Tape&Reel Information:5000pcs/Reel(Dimension in millimeter)**



產品別	EDFN 3x3
Reel尺寸	13"
編帶方式	
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後空格	50
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內/外箱比	10:01
外箱滿箱數	50K

★Datasheet Latest version specification :

	Revision History	Prepared	Approved	Date
A.0	Initial Datasheet	Johnson	Sam	2020/9/8