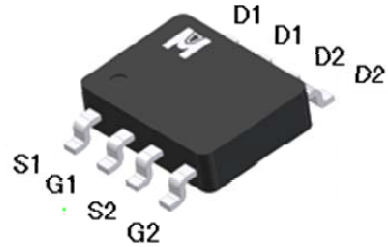
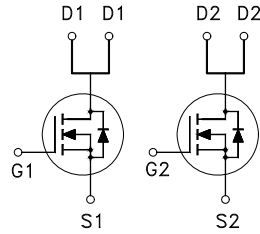


Dual N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	60V
$R_{DS(on)}$ (MAX.)	45m Ω
I_D	6A



UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_A = 25\text{ }^\circ\text{C}$	I_D	6	A
	$T_A = 100\text{ }^\circ\text{C}$		4.5	
Pulsed Drain Current ¹		I_{DM}	24	
Avalanche Current		I_{AS}	15	
Avalanche Energy	$L = 0.1\text{mH}, I_D = 12\text{A}, R_G = 25\Omega$	E_{AS}	7.2	mJ
Repetitive Avalanche Energy ²	$L = 0.05\text{mH}$	E_{AR}	3.6	
Power Dissipation	$T_A = 25\text{ }^\circ\text{C}$	P_D	2	W
	$T_A = 100\text{ }^\circ\text{C}$		0.8	
Operating Junction & Storage Temperature Range		T_{j}, T_{stg}	-55 to 150	$^\circ\text{C}$

100% UIS testing in condition of $V_D = 30\text{V}, L = 0.1\text{mH}, V_G = 10\text{V}, I_L = 10\text{A}$, Rated $V_{DS} = 60\text{V}$ N-CH

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		25	$^\circ\text{C} / \text{W}$
Junction-to-Ambient ³	$R_{\theta JA}$		62.5	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$

³62.5 $^\circ\text{C} / \text{W}$ when mounted on a 1 in² pad of 2 oz copper.



ELECTRICAL CHARACTERISTICS ($T_A = 25\text{ }^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	60			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.0	2.0	3.2	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 48V, V_{GS} = 0V$			1	μA
		$V_{DS} = 40V, V_{GS} = 0V, T_J = 125\text{ }^\circ\text{C}$			25	
On-State Drain Current ¹	$I_{D(ON)}$	$V_{DS} = 5V, V_{GS} = 10V$	5			A
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 6A$		40	45	$m\Omega$
		$V_{GS} = 5V, I_D = 5A$		55	70	
Forward Transconductance ¹	g_{fs}	$V_{DS} = 5V, I_D = 5A$		15		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = 30V, f = 1MHz$		945		pF
Output Capacitance	C_{oss}			81		
Reverse Transfer Capacitance	C_{rss}			56		
Total Gate Charge ^{1,2}	Q_g	$V_{DS} = 30V, V_{GS} = 10V,$ $I_D = 5A$		18		nC
Gate-Source Charge ^{1,2}	Q_{gs}			3.3		
Gate-Drain Charge ^{1,2}	Q_{gd}			5.1		
Turn-On Delay Time ^{1,2}	$t_{d(on)}$	$V_{DS} = 30V,$ $I_D = 1A, V_{GS} = 10V, R_{GS} = 6\Omega$		12		nS
Rise Time ^{1,2}	t_r			8		
Turn-Off Delay Time ^{1,2}	$t_{d(off)}$			20		
Fall Time ^{1,2}	t_f			7		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_C = 25\text{ }^\circ\text{C}$)						
Continuous Current	I_S				2.3	A
Pulsed Current ³	I_{SM}				9.2	
Forward Voltage ¹	V_{SD}	$I_F = I_S, V_{GS} = 0V$			1.2	V

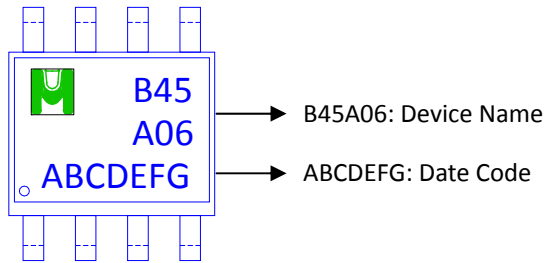
¹Pulse test : Pulse Width $\leq 300\ \mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

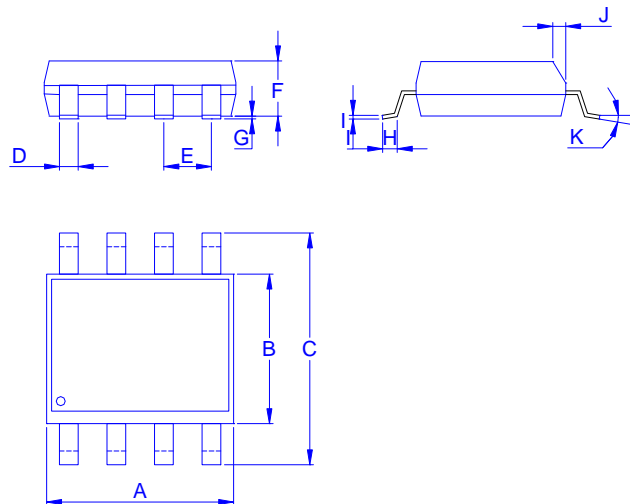
³Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: EMB45A06G for SOP-8



Outline Drawing



Dimension in mm

Dimension	A	B	C	D	E	F	G	H	I	J	K
Min.	4.70	3.70	5.80	0.33		1.20	0.08	0.40	0.19	0.25	0°
Typ.					1.27						
Max.	5.10	4.10	6.20	0.51		1.62	0.28	0.83	0.26	0.50	8°

