

P-Channel Logic Level Enhancement Mode Field Effect Transistor

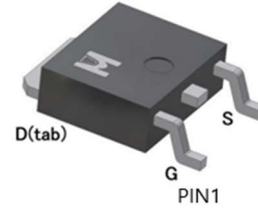
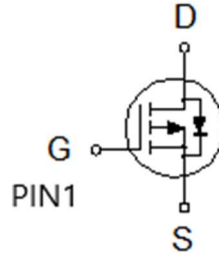
Product Summary:

BV_{DSS}	-40V
$R_{DS(on)}$ (MAX.)	44m Ω
I_D	-25A

P Channel MOSFET

UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ($T_c = 25\text{ }^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_c = 25\text{ }^\circ\text{C}$	I_D	-25	A
	$T_c = 100\text{ }^\circ\text{C}$		-16	
Pulsed Drain Current ¹		I_{DM}	-100	
Avalanche Current		I_{AS}	-23	
Avalanche Energy	L = 0.1mH	E_{AS}	26	mJ
Repetitive Avalanche Energy ²	L = 0.05mH	E_{AR}	13	
Power Dissipation	$T_c = 25\text{ }^\circ\text{C}$	P_D	50	W
	$T_c = 100\text{ }^\circ\text{C}$		20	
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		2.5	$^\circ\text{C}/\text{W}$
Junction-to-Ambient	$R_{\theta JA}$		75	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$



ELECTRICAL CHARACTERISTICS ($T_c = 25\text{ }^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-40			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-1	-2	-3	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -32V, V_{GS} = 0V$			-1	μA
		$V_{DS} = -30V, V_{GS} = 0V, T_J = 125\text{ }^\circ\text{C}$			-25	
On-State Drain Current ¹	$I_{D(ON)}$	$V_{DS} = -5V, V_{GS} = -4.5V$	-25			A
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = -10V, I_D = -10A$		38	44	m Ω
		$V_{GS} = -4.5V, I_D = -6A$		60	75	
Forward Transconductance ¹	g_{fs}	$V_{DS} = -5V, I_D = -10A$		11		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = -20V, f = 1MHz$		745		pF
Output Capacitance	C_{oss}			78		
Reverse Transfer Capacitance	C_{rss}			58		
Gate Resistance	R_g	$V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz$		5.8		Ω
Total Gate Charge ^{1,2}	Q_g	$V_{DS} = -10V, V_{GS} = -10V,$ $I_D = -6A$		11.5		nC
Gate-Source Charge ^{1,2}	Q_{gs}			2.5		
Gate-Drain Charge ^{1,2}	Q_{gd}			2.8		
Turn-On Delay Time ^{1,2}	$t_{d(on)}$	$V_{DS} = -10V,$ $I_D = -1A, V_{GS} = -10V, R_{GS} = 6\Omega$		7		nS
Rise Time ^{1,2}	t_r			10		
Turn-Off Delay Time ^{1,2}	$t_{d(off)}$			20		
Fall Time ^{1,2}	t_f			12		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_c = 25\text{ }^\circ\text{C}$)						
Continuous Current	I_S				-20	A
Pulsed Current ³	I_{SM}				-80	
Forward Voltage ¹	V_{SD}	$I_F = I_S, V_{GS} = 0V$			1.3	V
Reverse Recovery Time	t_{rr}	$I_F = -5A, dI_F/dt = 100A / \mu S$		15		nS
Reverse Recovery Charge	Q_{rr}			8		nC

¹Pulse test : Pulse Width $\leq 300\text{ }\mu\text{sec}$, Duty Cycle $\leq 2\%$.

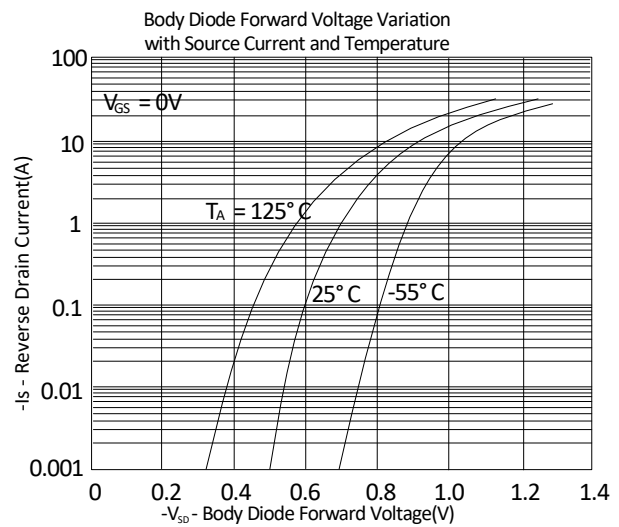
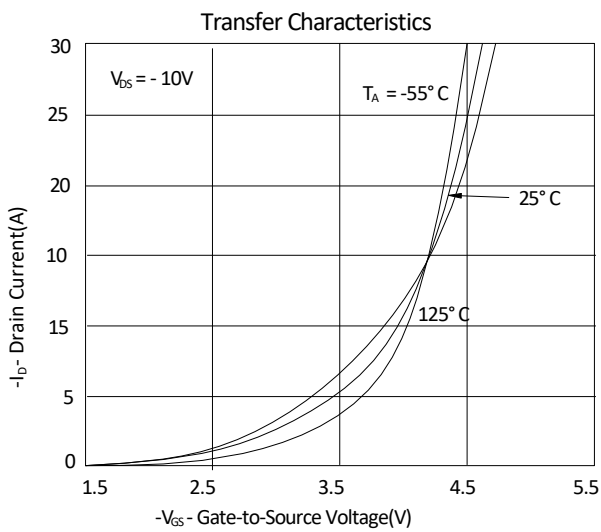
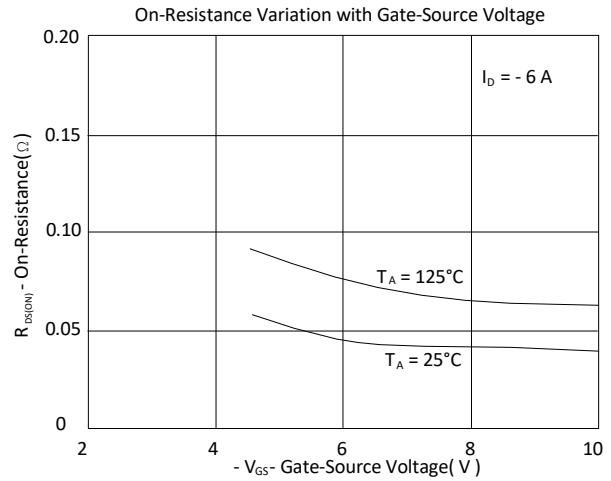
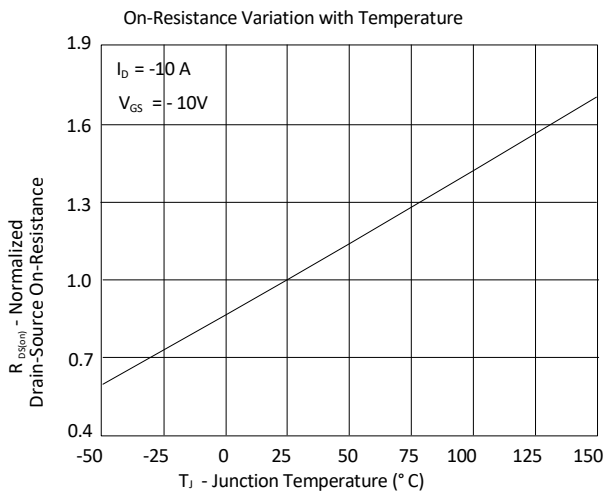
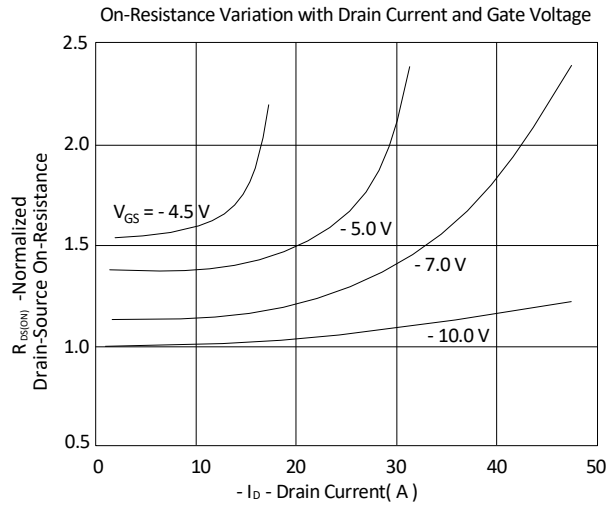
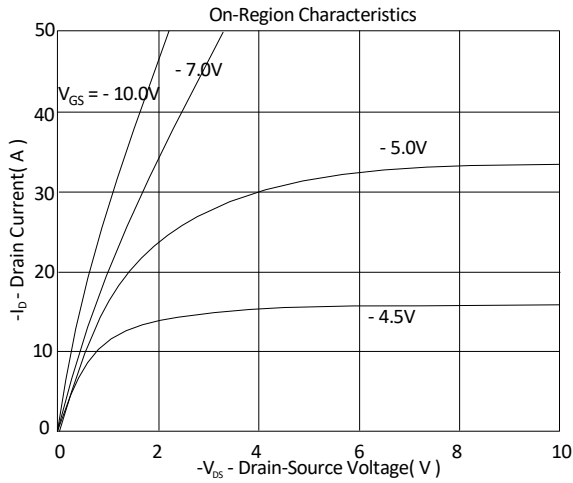
²Independent of operating temperature.

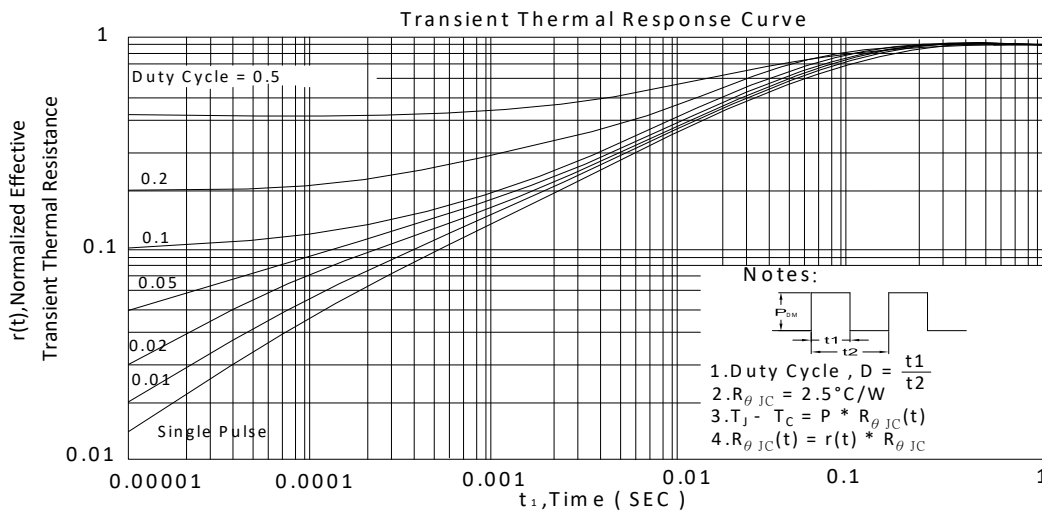
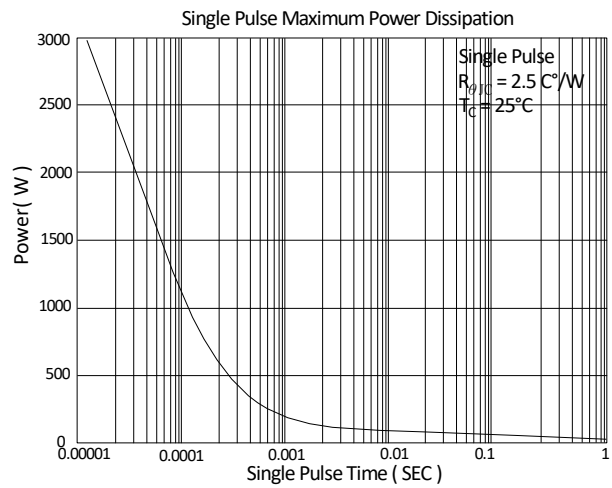
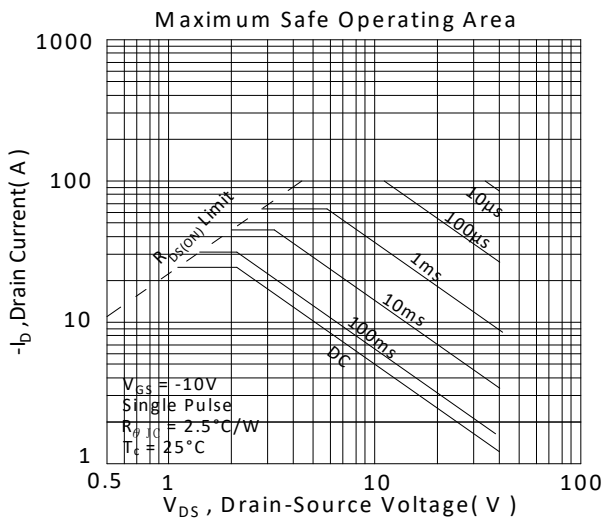
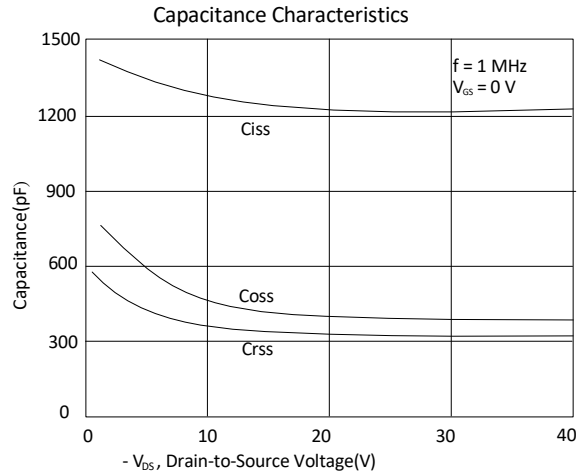
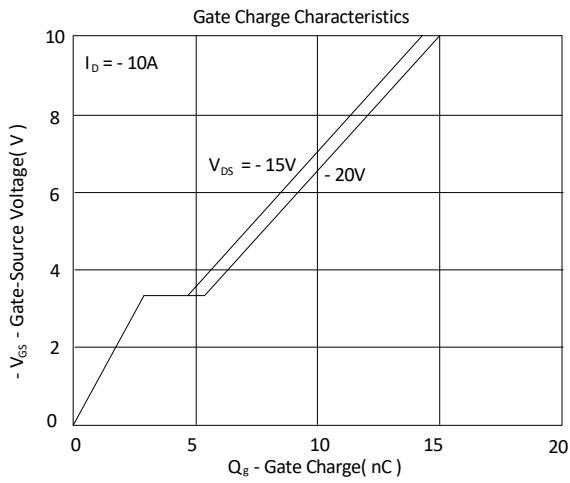
³Pulse width limited by maximum junction temperature.

EMC will review datasheet by quarter, and update new version.



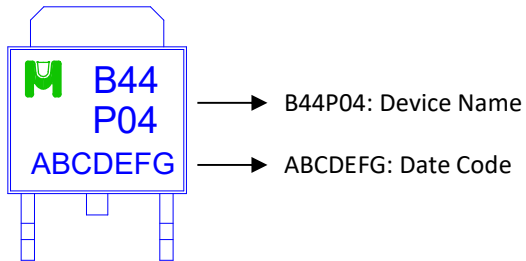
TYPICAL CHARACTERISTICS



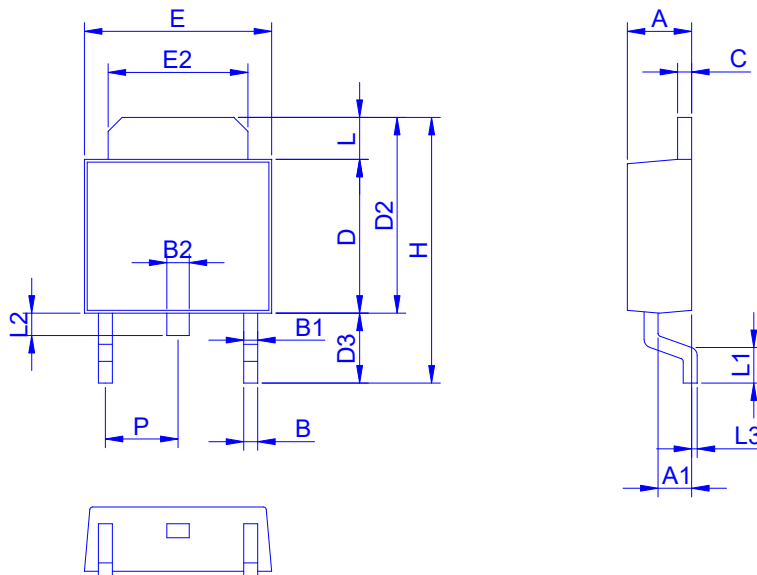


Ordering & Marking Information:

Device Name: EMB44P04A for DPAK (TO-252)

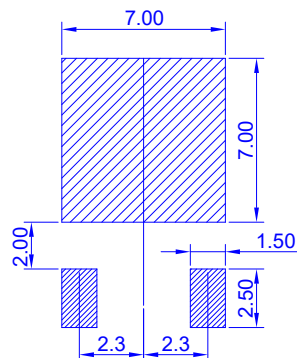


Outline Drawing



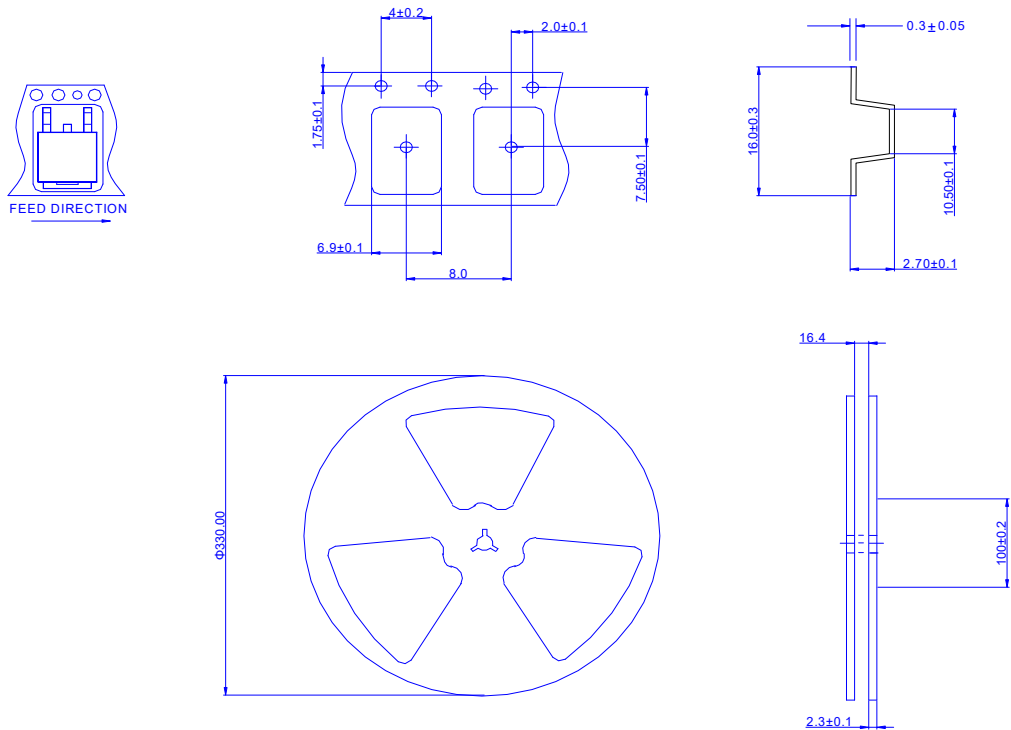
Dimension	A	A1	B	B1	B2	C	D	D2	D3	E	E2	H	L	L1	L2	L3	P
Min.	2.10	0.95	0.30	0.40	0.60	0.40	5.30	6.70	2.20	6.40	4.80	9.20	0.89	0.90	0.50	0.00	2.10
Max.	2.50	1.30	0.85	0.94	1.00	0.60	6.20	7.30	3.00	6.70	5.45	10.15	1.70	1.65	1.10	0.30	2.50


Footprint





◆ Tape&Reel Information:2500pcs/Reel(Dimension in millimeter)



產品別	TO252-2
Reel 尺寸	13"
編帶方式	FEED DIRECTION → 
前空格	35
後空格	35
裝箱數	
滿捲數量	2.5K
捲/內盒比	1 : 1
內盒滿箱數	2.5K
內/外箱比	10 : 1
外箱滿箱數	25K