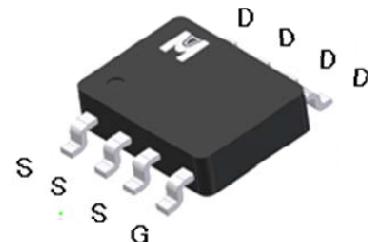
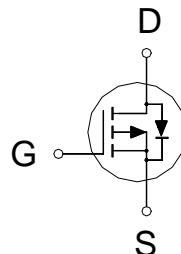


P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV _{DSS}	-60V
R _{DSON} (MAX.)	40mΩ
I _D	-7.5A



UIS, R_G 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V _{GS}	±20	V
Continuous Drain Current	T _A = 25 °C	I _D	-7.5	A
	T _A = 100 °C		-5	
Pulsed Drain Current ¹		I _{DM}	-30	
Avalanche Current		I _{AS}	-5	
Avalanche Energy	L = 0.1mH, ID=-5A, RG=25Ω	E _{AS}	1.25	mJ
Repetitive Avalanche Energy ²	L = 0.05mH	E _{AR}	0.625	
Power Dissipation	T _A = 25 °C	P _D	2.5	W
	T _A = 100 °C		1	
Operating Junction & Storage Temperature Range		T _j , T _{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	R _{θJC}	25	50	°C / W
Junction-to-Ambient	R _{θJA}			

¹Pulse width limited by maximum junction temperature.

²Duty cycle ≤ 1%

ELECTRICAL CHARACTERISTICS ($T_c = 25^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{GS} = 0V, I_D = -250\mu\text{A}$	-60			V
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$	-1.0	-1.8	-3.0	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -48V, V_{GS} = 0V$			-1	μA
		$V_{DS} = -40V, V_{GS} = 0V, T_J = 125^\circ\text{C}$			-25	
On-State Drain Current ¹	$I_{D(\text{ON})}$	$V_{DS} = -5V, V_{GS} = -10V$	-5			A
Drain-Source On-State Resistance ¹	$R_{DS(\text{ON})}$	$V_{GS} = -10V, I_D = -7.5\text{A}$		35	40	$\text{m}\Omega$
		$V_{GS} = -4.5V, I_D = -5\text{A}$		45	55	
Forward Transconductance ¹	g_{fs}	$V_{DS} = -5V, I_D = -7.5\text{A}$		30		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = -25V, f = 1\text{MHz}$		2975		pF
Output Capacitance	C_{oss}			240		
Reverse Transfer Capacitance	C_{rss}			150		
Gate Resistance	R_g	$V_{GS} = 15\text{mV}, V_{DS} = 0V, f = 1\text{MHz}$		6.5		Ω
Total Gate Charge ^{1,2}	Q_g	$V_{DS} = -30V, V_{GS} = -10V, I_D = -7.5\text{A}$		45		nC
Gate-Source Charge ^{1,2}	Q_{gs}			6		
Gate-Drain Charge ^{1,2}	Q_{gd}			7.5		
Turn-On Delay Time ^{1,2}	$t_{d(\text{on})}$	$V_{DS} = -10V, I_D = -1\text{A}, V_{GS} = -10V, R_{GS} = 6\Omega$		12		nS
Rise Time ^{1,2}	t_r			15		
Turn-Off Delay Time ^{1,2}	$t_{d(\text{off})}$			40		
Fall Time ^{1,2}	t_f			20		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_c = 25^\circ\text{C}$)						
Continuous Current	I_S				-2.3	A
Pulsed Current ³	I_{SM}				-9.2	
Forward Voltage ¹	V_{SD}	$I_F = I_S, V_{GS} = 0V$			-1.3	V

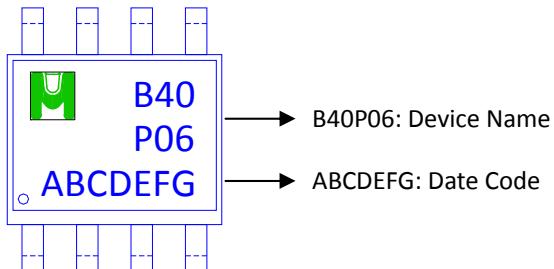
¹Pulse test : Pulse Width $\leq 300 \mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

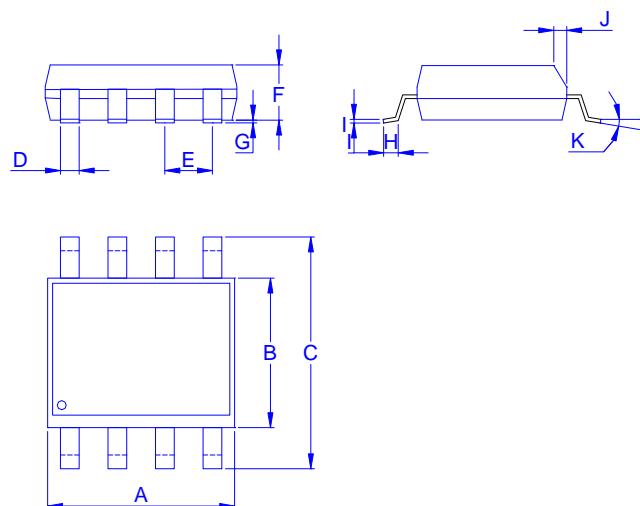
³Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: EMB40P06G for SOP-8



Outline Drawing



Dimension in mm

Dimension	A	B	C	D	E	F	G	H	I	J	K
Min.	4.70	3.70	5.80	0.33		1.20	0.08	0.40	0.19	0.25	0°
Typ.					1.27						
Max.	5.10	4.10	6.20	0.51		1.62	0.28	0.83	0.26	0.50	8°

TYPICAL CHARACTERISTICS

