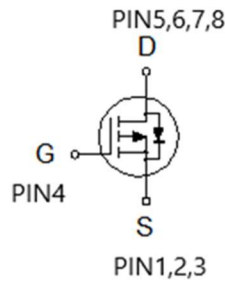


P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV _{DSS}	-40V
R _{DS(on)} (MAX.)	16mΩ
I _D	-20A



P-Channel MOSFET

UIS, R_g 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V _{GS}	±20	V
Continuous Drain Current	T _C = 25 °C	I _D	-20	A
	T _A = 25 °C		-10	
	T _C = 100 °C		-13	
Pulsed Drain Current ¹		I _{DM}	-80	
Avalanche Current		I _{AS}	-15	
Avalanche Energy	L = 0.1mH, I _{AS} = -15A, R _G = 25Ω	E _{AS}	11.25	mJ
Repetitive Avalanche Energy ²	L = 0.05mH	E _{AR}	5.62	
Power Dissipation	T _C = 25 °C	P _D	21	W
	T _C = 100 °C		8.3	
Power Dissipation	T _A = 25 °C	P _D	2.5	W
	T _A = 100 °C		1	
Operating Junction & Storage Temperature Range		T _J , T _{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	R _{θJC}		6	°C / W
Junction-to-Ambient ³	R _{θJA}		50	

¹Pulse width limited by maximum junction temperature.

²Duty cycle ≤ 1%



³50°C / W when mounted on a 1 in² pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = -250μA	-40			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250μA	-1.0	-1.8	-3.2	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -32V, V _{GS} = 0V			-1	μA
		V _{DS} = -30V, V _{GS} = 0V, T _J = 125 °C			-10	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = -5V, V _{GS} = -10V	-20			A
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = -10V, I _D = -10A		14	16	mΩ
		V _{GS} = -4.5V, I _D = -8A		32	40	
Forward Transconductance ¹	g _{fs}	V _{DS} = -5V, I _D = -10A		24		S
DYNAMIC						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = -20V, f = 1MHz		2950		pF
Output Capacitance	C _{oss}			287		
Reverse Transfer Capacitance	C _{rss}			250		
Gate Resistance	R _g	V _{GS} = 15mV, V _{DS} = 0V, f = 1MHz		4.0		Ω
Total Gate Charge ^{1,2}	Q _g	V _{DS} = -10V, V _{GS} = -10V, I _D = -10A		45.4		nC
Gate-Source Charge ^{1,2}	Q _{gs}			6.2		
Gate-Drain Charge ^{1,2}	Q _{gd}			8.2		
Turn-On Delay Time ^{1,2}	t _{d(on)}	V _{DS} = -15V, I _D = -1A, V _{GS} = -10V, R _{GS} = 2.7Ω		12		nS
Rise Time ^{1,2}	t _r			25		
Turn-Off Delay Time ^{1,2}	t _{d(off)}			30		
Fall Time ^{1,2}	t _f			24		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I _S				-20	A
Pulsed Current ³	I _{SM}				-80	
Forward Voltage ¹	V _{SD}	I _F = -10A, V _{GS} = 0V			-1.2	V
Reverse Recovery Time	t _{rr}	I _F = I _S , dI _F /dt = 100A / μS		30		nS
Reverse Recovery Charge	Q _{rr}			25		nC

¹Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.



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Excelliance MOS Corporation

EMB16P04V

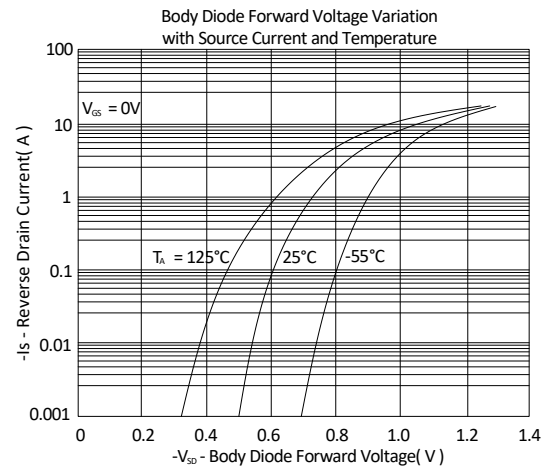
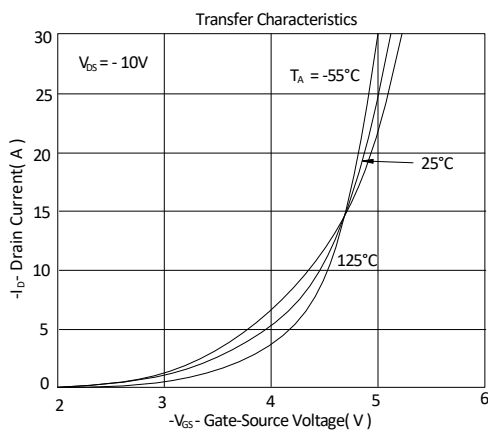
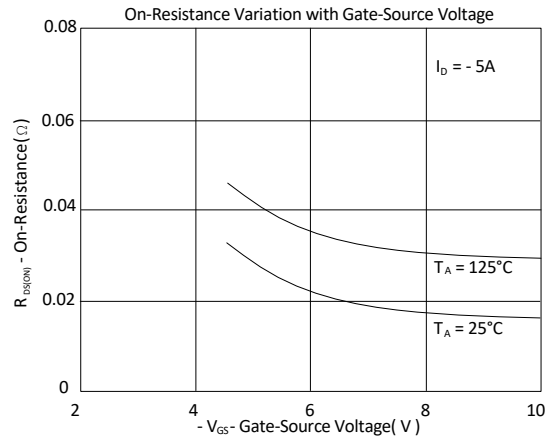
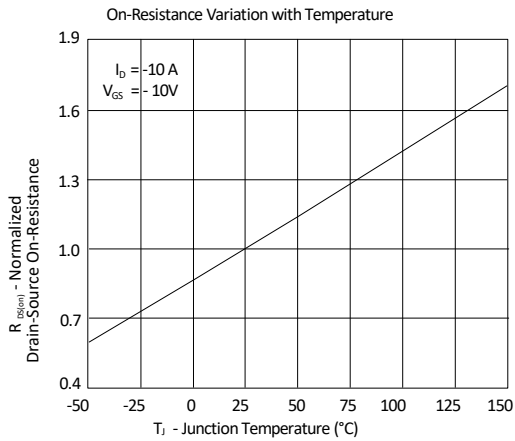
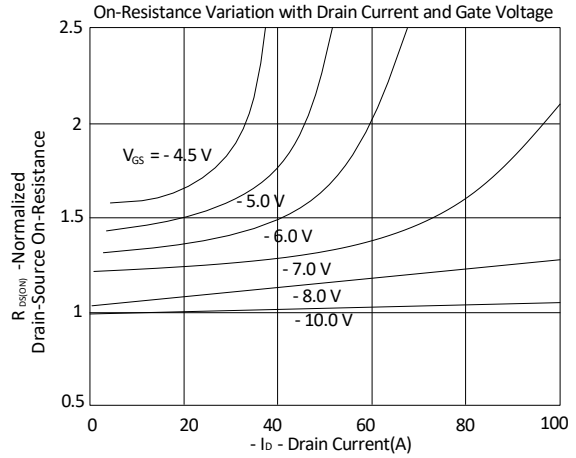
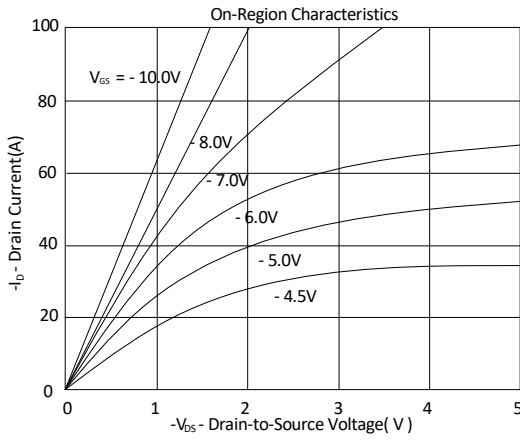
²Independent of operating temperature.

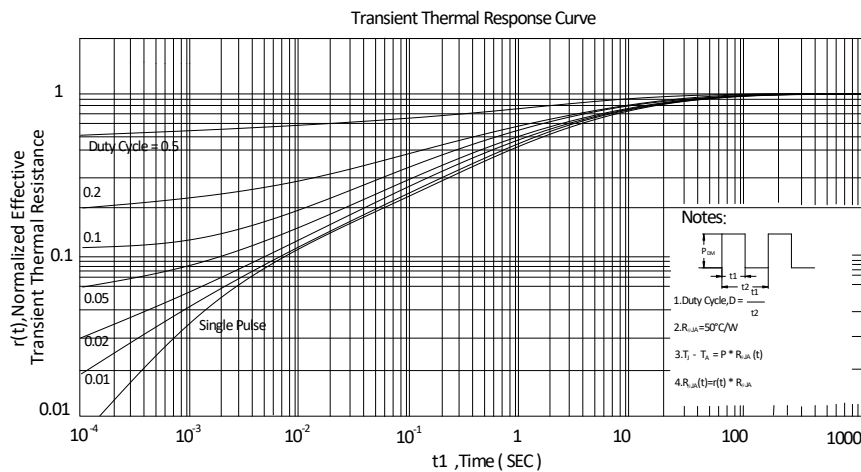
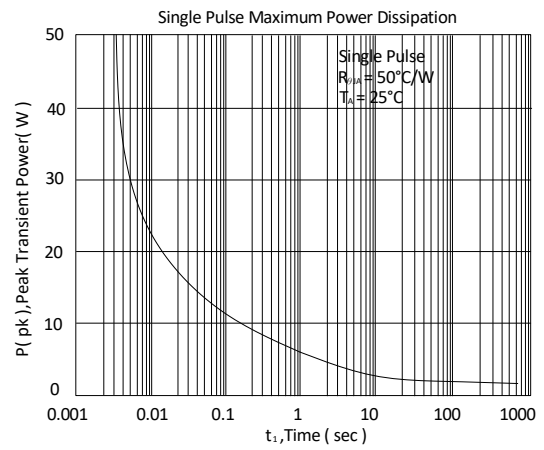
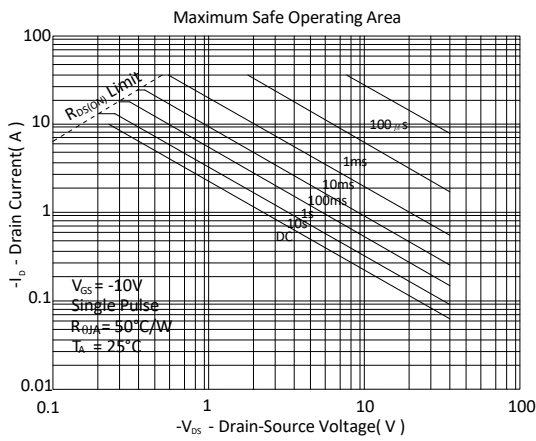
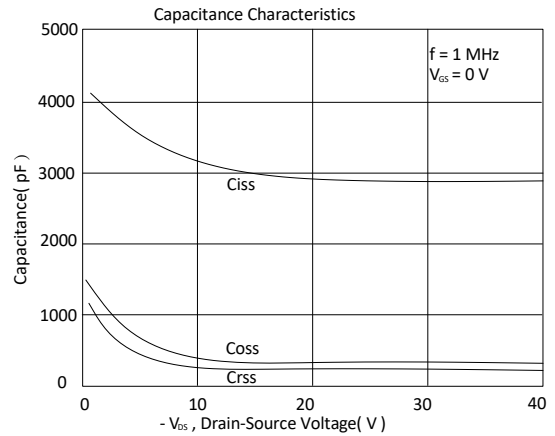
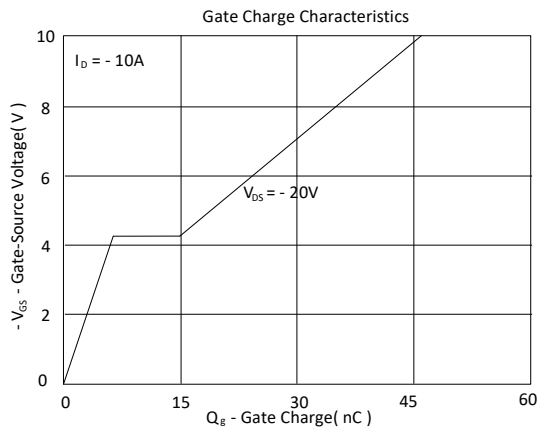
³Pulse width limited by maximum junction temperature.

EMC will review datasheet by quarter, and update new version.



TYPICAL CHARACTERISTICS





Ordering & Marking Information:

Device Name: EMB16P04V for EDFN 3 x 3



B16P04: Device Name

ABCDEFG: Date Code

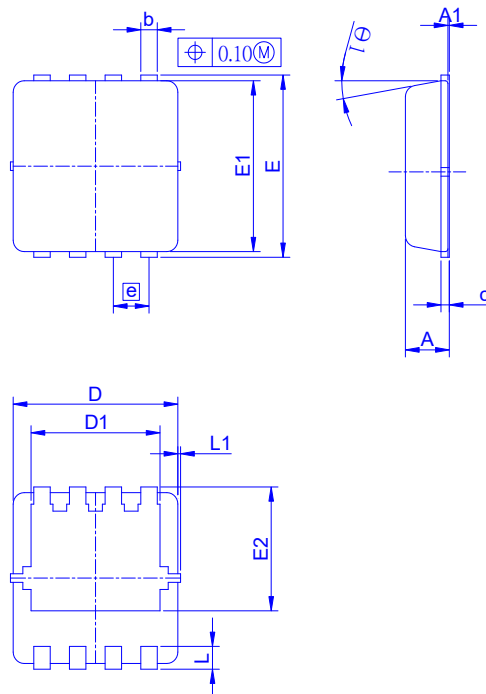
A: Assembly House

B: Year(A:2008 B:2009 C:2010....)

C: Month(A:01 B:02 C:03 D:04 E:05 F:06 G:07 H:08 I:09 J:10 K:11 L:12)

DEFG: Serial No.

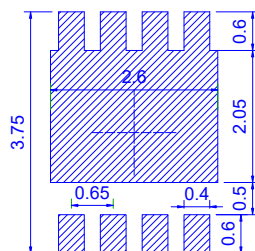
Outline Drawing



Dimension in mm

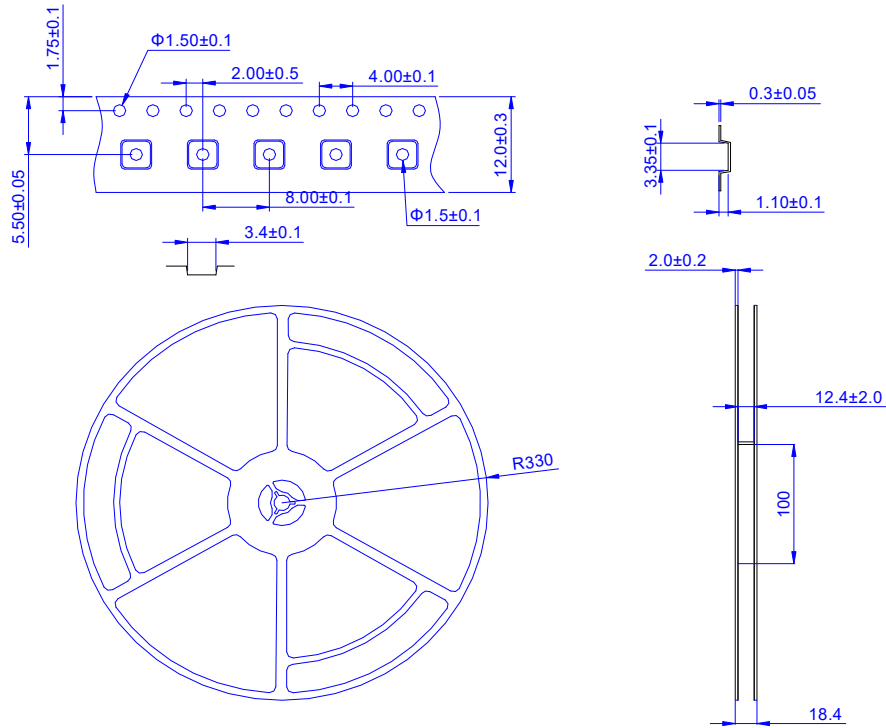
Dimension	A	A1	b	c	D	D1	E	E1	E2	e	L	L1	θ1
Min.	0.65	0	0.20	0.10	2.90	2.15	3.10	2.90	1.53	0.55	0.25	-	0°
Typ.	0.75	-	0.30	0.15	3.00	2.45	3.20	3.00	1.97	0.65	0.40	0.075	10°
Max.	0.90	0.05	0.40	0.25	3.30	2.74	3.50	3.30	2.59	0.75	0.60	0.150	14°

Recommended minimum pads





Tape&Reel Information: 5000pcs/Reel



產品別	EDFN3X3
Reel 尺寸	13"
編帶方式	<p>FEED DIRECTION</p>
前空格	50
後空格	50
裝箱數	
滿捲數量	5K
捲/內盒比	1 : 1
內盒滿箱數	5K
內/外箱比	10 : 1
外箱滿箱數	50K