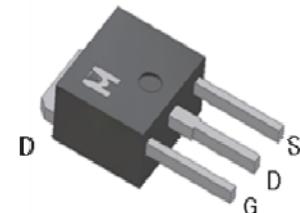
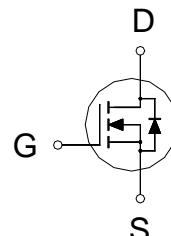


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV _{DSS}	30V
R _{DSON} (MAX.)	9mΩ
I _D	50A



UIS, R_G 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V _{GS}	±20	V
Continuous Drain Current	T _C = 25 °C	I _D	50	A
	T _C = 100 °C		35	
Pulsed Drain Current ¹		I _{DM}	140	
Avalanche Current		I _{AS}	37.5	
Avalanche Energy	L = 0.1mH, ID=37.5A, RG=25Ω	E _{AS}	70	mJ
Repetitive Avalanche Energy ²	L = 0.05mH	E _{AR}	15	
Power Dissipation	T _C = 25 °C	P _D	50	W
	T _C = 100 °C		20	
Operating Junction & Storage Temperature Range		T _j , T _{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	R _{θJC}	2.5	2.5	°C / W
Junction-to-Ambient	R _{θJA}		75	

¹Pulse width limited by maximum junction temperature.

²Duty cycle ≤ 1%

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0\text{V}, I_D = 250\mu\text{A}$	30			V
Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{DS}} = V_{\text{GS}}, I_D = 250\mu\text{A}$	1	1.7	3	
Gate-Body Leakage	I_{GSS}	$V_{\text{DS}} = 0\text{V}, V_{\text{GS}} = \pm 20\text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{DS}} = 24\text{V}, V_{\text{GS}} = 0\text{V}$			1	μA
		$V_{\text{DS}} = 20\text{V}, V_{\text{GS}} = 0\text{V}, T_J = 125^\circ\text{C}$			25	
On-State Drain Current ¹	$I_{\text{D}(\text{ON})}$	$V_{\text{DS}} = 10\text{V}, V_{\text{GS}} = 10\text{V}$	50			A
Drain-Source On-State Resistance ¹	$R_{\text{DS}(\text{ON})}$	$V_{\text{GS}} = 10\text{V}, I_D = 25\text{A}$		7.5	9	$\text{m}\Omega$
		$V_{\text{GS}} = 4.5\text{V}, I_D = 15\text{A}$		11	13.5	
Forward Transconductance ¹	g_{fs}	$V_{\text{DS}} = 5\text{V}, I_D = 20\text{A}$		20		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{\text{GS}} = 0\text{V}, V_{\text{DS}} = 15\text{V}, f = 1\text{MHz}$		828		pF
Output Capacitance	C_{oss}			196		
Reverse Transfer Capacitance	C_{rss}			174		
Gate Resistance	R_g	$V_{\text{GS}} = 15\text{mV}, V_{\text{DS}} = 0\text{V}, f = 1\text{MHz}$		1.7		Ω
Total Gate Charge ^{1,2}	$Q_g(V_{\text{GS}}=10\text{V})$	$V_{\text{DS}} = 15\text{V}, V_{\text{GS}} = 10\text{V}, I_D = 25\text{A}$		17.6		nC
	$Q_g(V_{\text{GS}}=4.5\text{V})$			12.5		
Gate-Source Charge ^{1,2}	Q_{gs}			2.8		
Gate-Drain Charge ^{1,2}	Q_{gd}			7.4		
Turn-On Delay Time ^{1,2}	$t_{d(\text{on})}$	$V_{\text{DS}} = 15\text{V}, I_D = 25\text{A}, V_{\text{GS}} = 10\text{V}, R_{\text{GS}} = 2.7\Omega$		8		ns
Rise Time ^{1,2}	t_r			18		
Turn-Off Delay Time ^{1,2}	$t_{d(\text{off})}$			20		
Fall Time ^{1,2}	t_f			3		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_c = 25^\circ\text{C}$)						
Continuous Current	I_S	$I_F = I_S, V_{\text{GS}} = 0\text{V}$			50	A
Pulsed Current ³	I_{SM}				140	
Forward Voltage ¹	V_{SD}				1.3	
Reverse Recovery Time	t_{rr}			22		
Peak Reverse Recovery Current	$I_{\text{RM}(\text{REC})}$			180		
Reverse Recovery Charge	Q_{rr}			12		

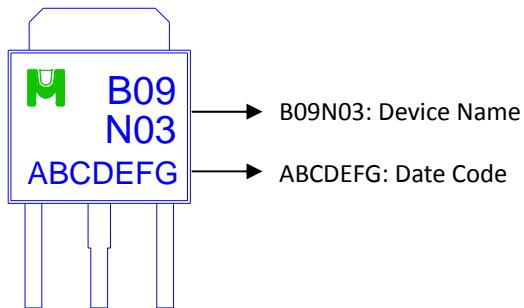
¹Pulse test : Pulse Width \leq 300 μ sec, Duty Cycle \leq 2%.

²Independent of operating temperature.

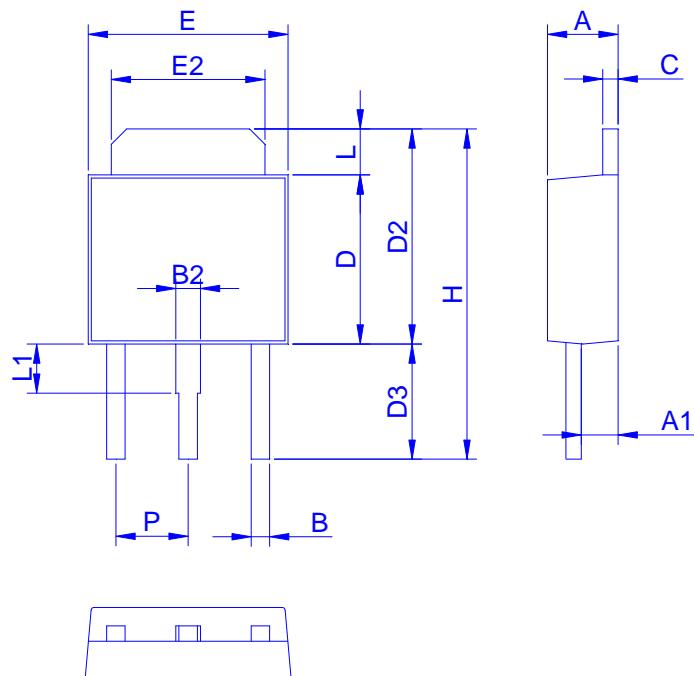
³Pulse width limited by maximum junction temperature.

Ordering & Marking Information:

Device Name: EMB09N03CS for IPAK (TO-251)



Outline Drawing



Dimension in mm

Dimension	A	A1	B	B2	C	D	D2	D3	E	E2	H	L	L1	P
Min.	2.10	0.90	0.40	0.60	0.40	5.30	6.70	3.40	6.30	4.80	10.2	0.89	0.90	2.10
Max.	2.50	1.50	0.90	1.15	0.60	6.25	7.30	4.30	6.80	5.50	11.5	1.40	1.80	2.50

TYPICAL CHARACTERISTICS

