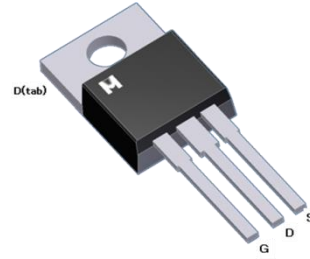
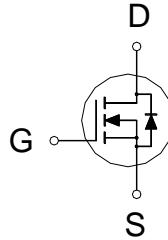


N-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV _{DSS}	60V
R _{DS(on)} (MAX.)	4mΩ
I _D	165A



UIS, R_g 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V _{GS}	±20	V
Continuous Drain Current	T _C = 25 °C	I _D	165	A
	T _C = 100 °C		104	
Pulsed Drain Current ^{1,3}		I _{DM}	540	
Avalanche Current		I _{AS}	65	
Avalanche Energy	L = 0.1mH, I _{AS} =65A, R _G =25Ω	E _{AS}	211	mJ
Repetitive Avalanche Energy ²	L = 0.05mH	E _{AR}	105	
Power Dissipation	T _C = 25 °C	P _D	192	W
	T _C = 100 °C		76	
Operating Junction & Storage Temperature Range		T _j , T _{stg}	-55 to 150	°C

100% UIS testing in condition of V_D=30V, L=0.1mH, V_G=10V, I_L=40A, Rated V_{DS}=60V N-CH

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	R _{θJC}		0.65	°C / W
Junction-to-Ambient	R _{θJA}		62.5	

¹Pulse width limited by maximum junction temperature.

²Duty cycle ≤ 1%

³Pulsed drain current rating is package limited.



ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^\circ\text{C}$, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	60			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.0	1.8	2.5	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 48V, V_{GS} = 0V$			1	μA
		$V_{DS} = 40V, V_{GS} = 0V, T_J = 125\text{ }^\circ\text{C}$			25	
On-State Drain Current ¹	$I_{D(ON)}$	$V_{DS} = 5V, V_{GS} = 10V$	165			A
Drain-Source On-State Resistance ¹	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 20A$		3.3	4.0	$m\Omega$
		$V_{GS} = 4.5V, I_D = 20A$		4.4	5.5	
Forward Transconductance ¹	g_{fs}	$V_{DS} = 5V, I_D = 20A$		58		S
DYNAMIC						
Input Capacitance	C_{iss}	$V_{GS} = 0V, V_{DS} = 30V, f = 1MHz$		3250		pF
Output Capacitance	C_{oss}			1200		
Reverse Transfer Capacitance	C_{rss}			50		
Gate Resistance	R_g	$V_{GS} = 15mV, V_{DS} = 0V, f = 1MHz$		1.6		Ω
Total Gate Charge ^{1,2}	Q_g	$V_{DS} = 30V, V_{GS} = 10V,$ $I_D = 20A$		49		nC
Gate-Source Charge ^{1,2}	Q_{gs}			8		
Gate-Drain Charge ^{1,2}	Q_{gd}			9		
Turn-On Delay Time ^{1,2}	$t_{d(on)}$	$V_{DS} = 30V,$ $I_D = 20A, V_{GS} = 10V, R_{GS} = 6\Omega$		12		nS
Rise Time ^{1,2}	t_r			10		
Turn-Off Delay Time ^{1,2}	$t_{d(off)}$			55		
Fall Time ^{1,2}	t_f			15		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ($T_C = 25\text{ }^\circ\text{C}$)						
Continuous Current	I_S				165	A
Pulsed Current ³	I_{SM}				540	
Forward Voltage ¹	V_{SD}	$I_F = 20A, V_{GS} = 0V$			1.2	V
Reverse Recovery Time	t_{rr}	$I_F = 20A, dI_F/dt = 300A / \mu S$		50		nS
Reverse Recovery Charge	Q_{rr}				120	

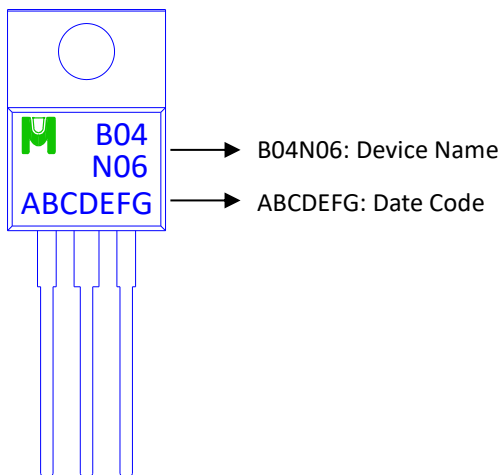
¹Pulse test : Pulse Width $\leq 300 \mu\text{sec}$, Duty Cycle $\leq 2\%$.

²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

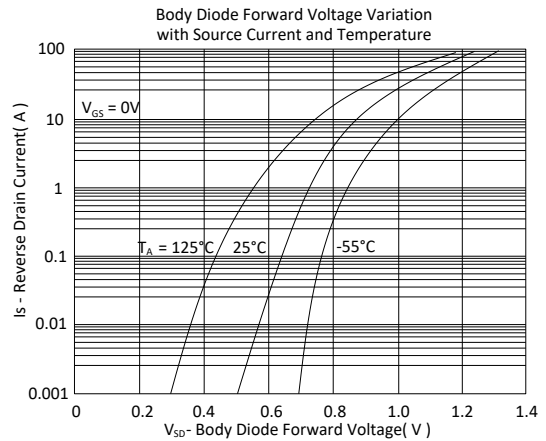
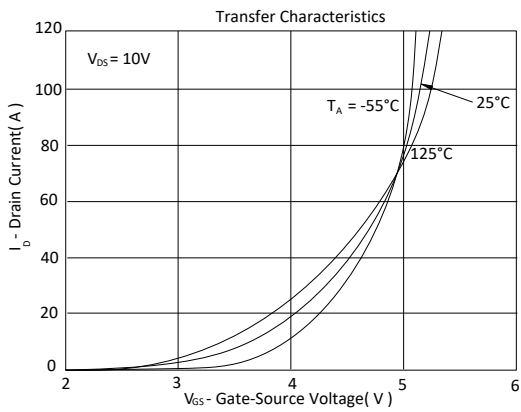
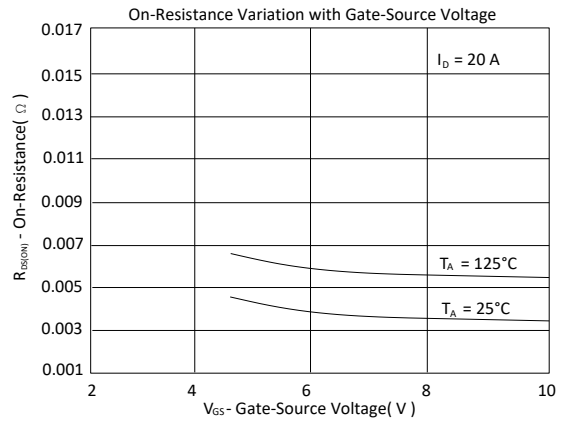
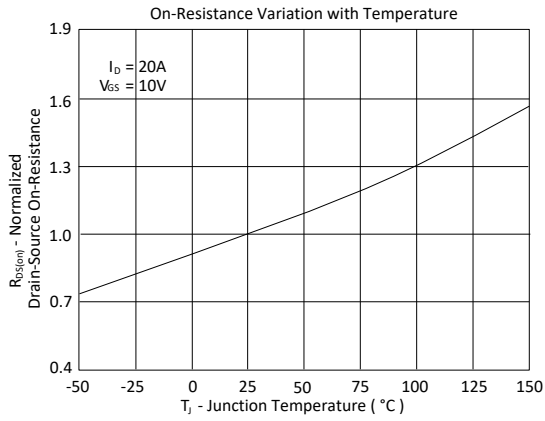
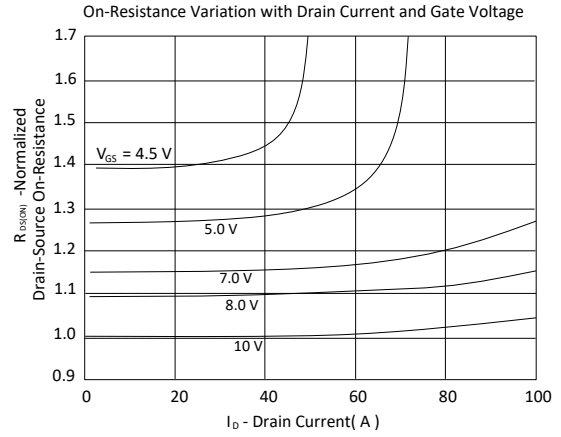
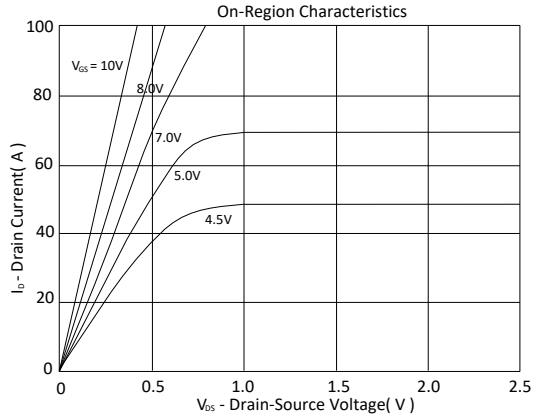
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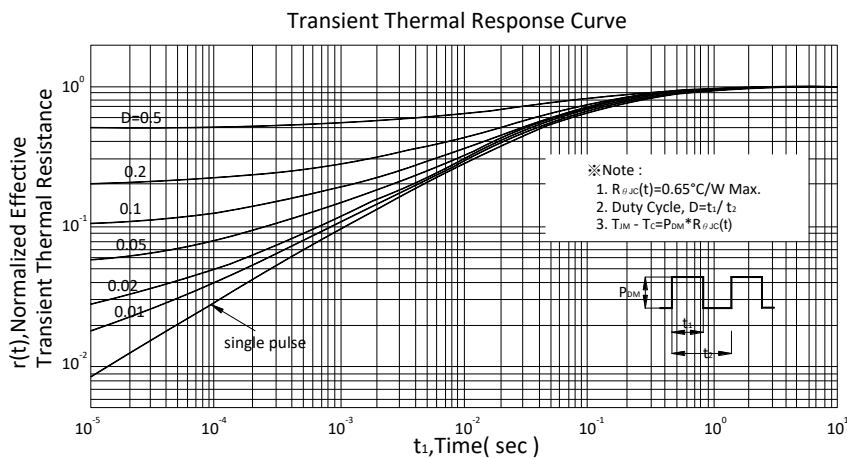
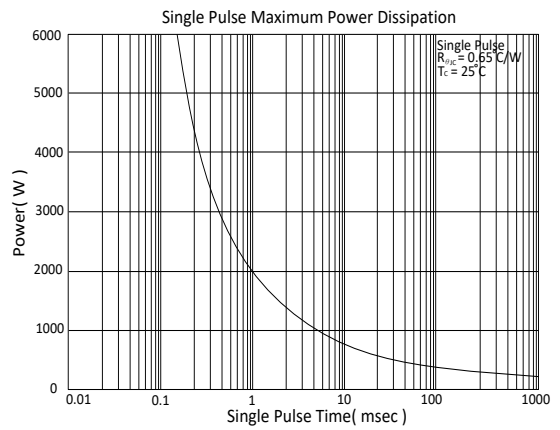
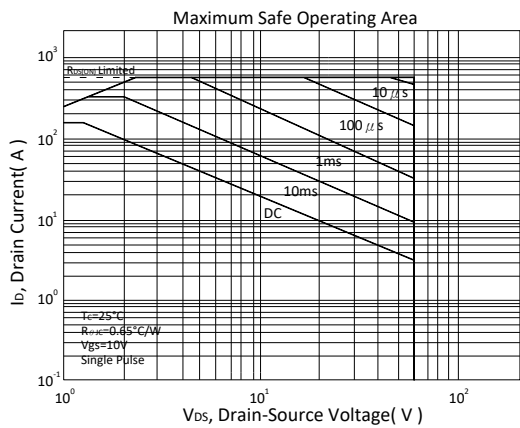
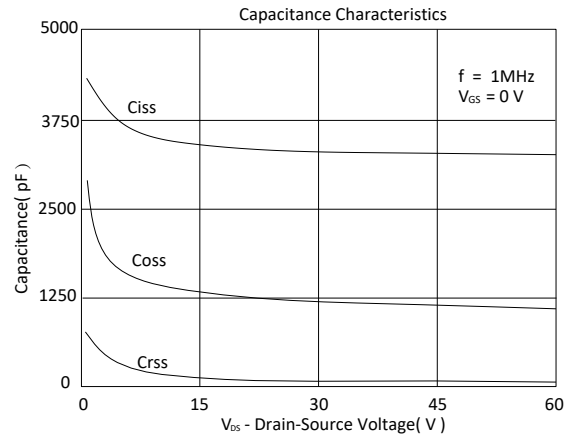
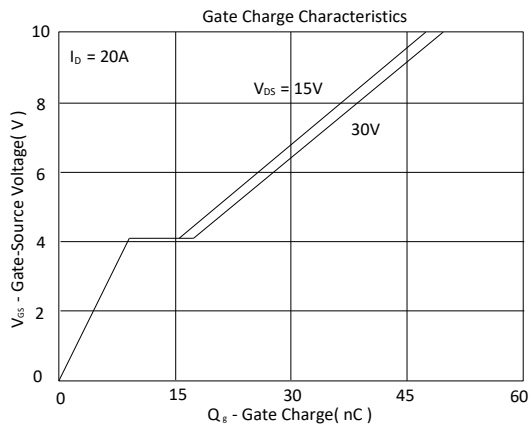
Device Name: EMB04N06E for TO-220





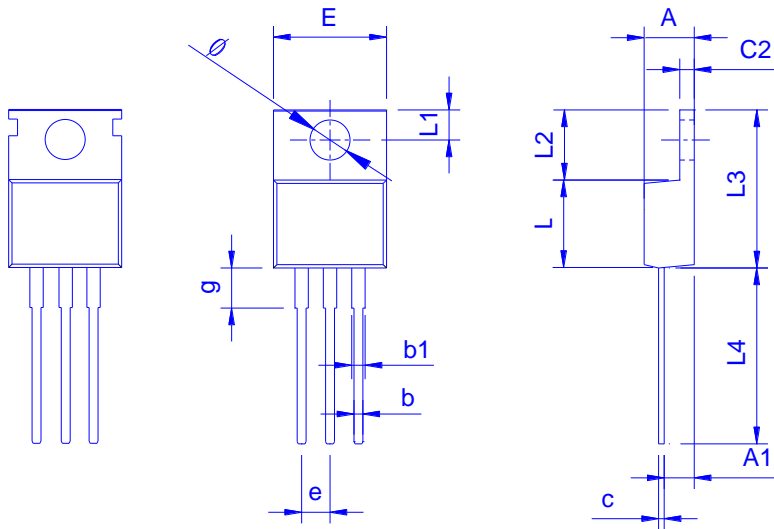
TYPICAL CHARACTERISTICS







Outline Drawing



Dimension in mm

Dimension	A	A1	b	b1	c	c2	E	L	L1	L2	L3	L4	φ	e	g
Min.	4.07	2.04	0.60	1.15	0.31	1.11	9.90	8.30	2.50	6.00	14.30	12.70	3.40	2.04	2.85
Typ.	4.44	2.40	0.80	1.27	-	1.27	10.16	-	2.74	6.30	15.00	13.40	3.84	2.54	3.71
Max.	4.82	3.00	1.00	1.75	0.65	1.41	11.50	9.75	3.25	6.80	16.90	14.50	4.00	3.04	4.10