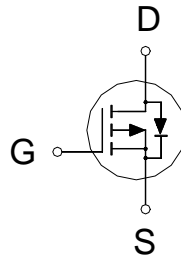


P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	-30V
$R_{DS(on) (MAX.)}$	3.1m Ω
I_D	-110A



P Channel MOSFET

UIS, Rg 100% Tested

Pb-Free Lead Plating & Halogen Free



ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^\circ\text{C}$ Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_C = 25\text{ }^\circ\text{C}$	I_D	-110	A
	$T_C = 100\text{ }^\circ\text{C}$		-70	
Pulsed Drain Current ¹		I_{DM}	-440	
Avalanche Current		I_{AS}	-80	
Avalanche Energy	L = 0.1mH	E_{AS}	320	mJ
Repetitive Avalanche Energy ²	L = 0.05mH	E_{AR}	160	
Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	P_D	65	W
	$T_C = 100\text{ }^\circ\text{C}$		26	
Operating Junction & Storage Temperature Range		T_{j}, T_{stg}	-55 to 150	$^\circ\text{C}$

100% UIS testing in condition of $V_D=25\text{V}$, $L=0.1\text{mH}$, $V_G=10\text{V}$, $I_L=50\text{A}$, Rated $V_{DS}=30\text{V}$ P-CH

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	$R_{\theta JC}$		1.9	$^\circ\text{C} / \text{W}$
Junction-to-Ambient ³	$R_{\theta JA}$		62.5	

¹Pulse width limited by maximum junction temperature.

²Duty cycle $\leq 1\%$

³62.5 $^\circ\text{C} / \text{W}$ when mounted on a 1 in² pad of 2 oz copper.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C, Unless Otherwise Noted)

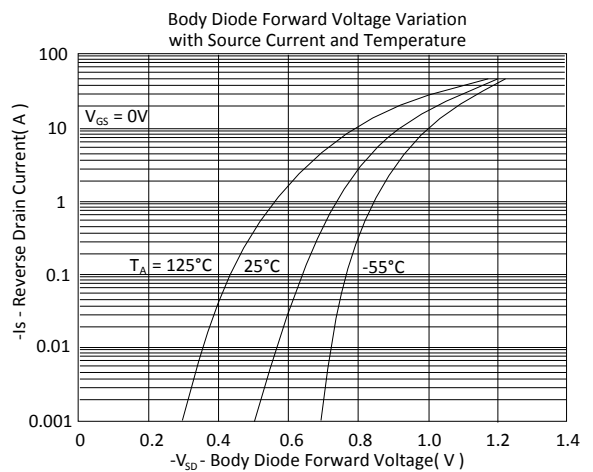
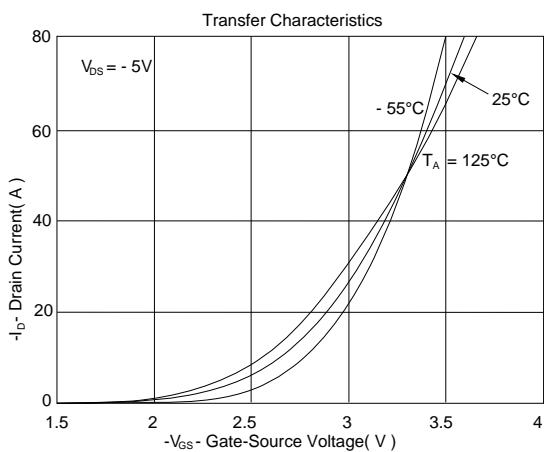
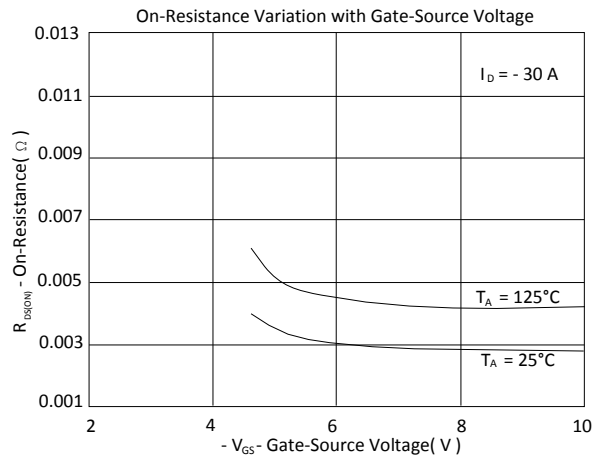
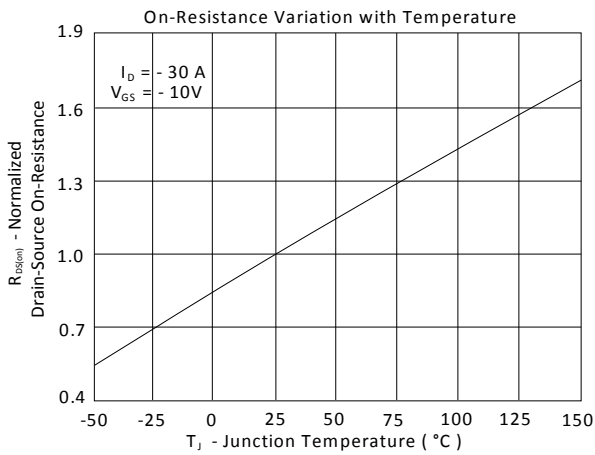
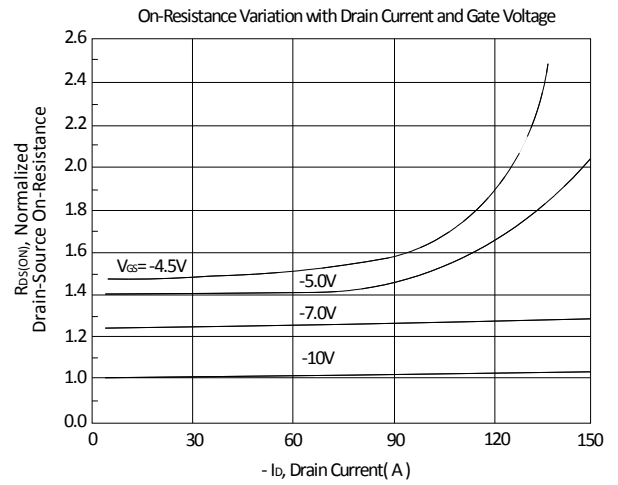
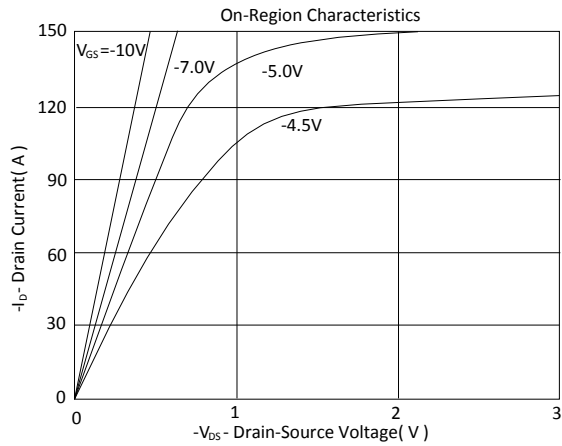
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = -250μA	-30			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250μA	-1	-1.5	-3	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0V, V _{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -24V, V _{GS} = 0V			-1	μA
		V _{DS} = -20V, V _{GS} = 0V, T _J = 125 °C			-10	
On-State Drain Current ¹	I _{D(ON)}	V _{DS} = -5V, V _{GS} = -10V	-85			A
Drain-Source On-State Resistance ¹	R _{DS(ON)}	V _{GS} = -10V, I _D = -30A		2.7	3.1	mΩ
		V _{GS} = -4.5V, I _D = -30A		4.0	5.0	
Forward Transconductance ¹	g _{fs}	V _{DS} = -5V, I _D = -30A		70		S
DYNAMIC						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = -15V, f = 1MHz		6400		pF
Output Capacitance	C _{oss}			913		
Reverse Transfer Capacitance	C _{rss}			656		
Gate Resistance	R _g	V _{GS} = 15mV, V _{DS} = 0V, f = 1MHz		3.4		Ω
Total Gate Charge ^{1,2}	Q _g	V _{DS} = -15V, V _{GS} = -10V, I _D = -30A		96.5		nC
Gate-Source Charge ^{1,2}	Q _{gs}			24.8		
Gate-Drain Charge ^{1,2}	Q _{gd}			13.8		
Turn-On Delay Time ^{1,2}	t _{d(on)}	V _{DS} = -15V, I _D = -1A, V _{GS} = -10V, R _{GS} = 2.7Ω		15		nS
Rise Time ^{1,2}	t _r			20		
Turn-Off Delay Time ^{1,2}	t _{d(off)}			130		
Fall Time ^{1,2}	t _f			55		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I _S				-85	A
Pulsed Current ³	I _{SM}				-260	
Forward Voltage ¹	V _{SD}	I _F = -30A, V _{GS} = 0V			-1.2	V
Reverse Recovery Time	t _{rr}	I _F = I _S , dI _F /dt = 100A / μS		26		nS
Reverse Recovery Charge	Q _{rr}			80		nC

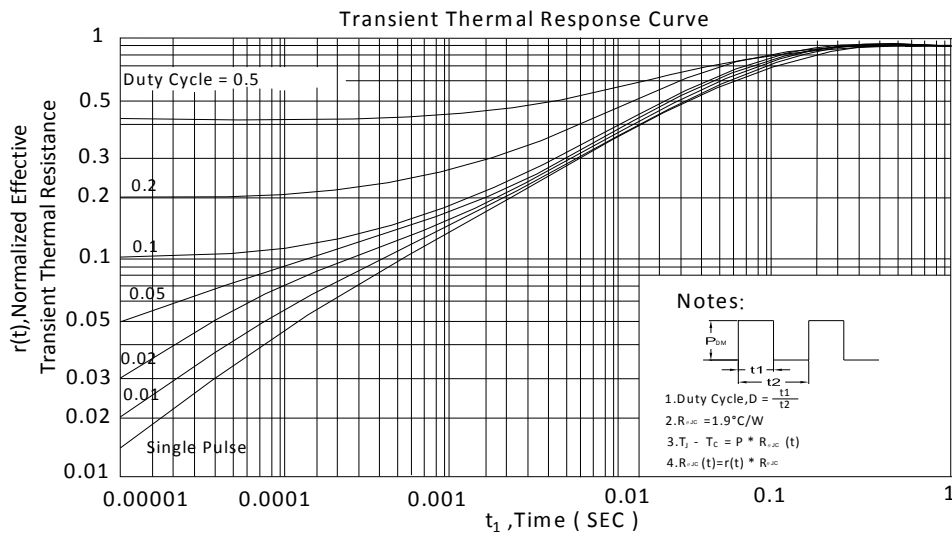
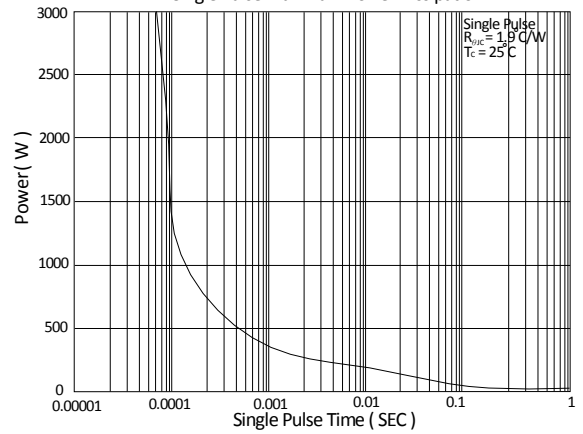
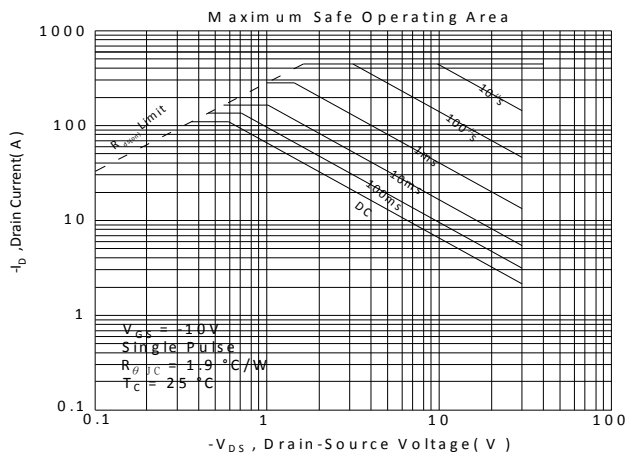
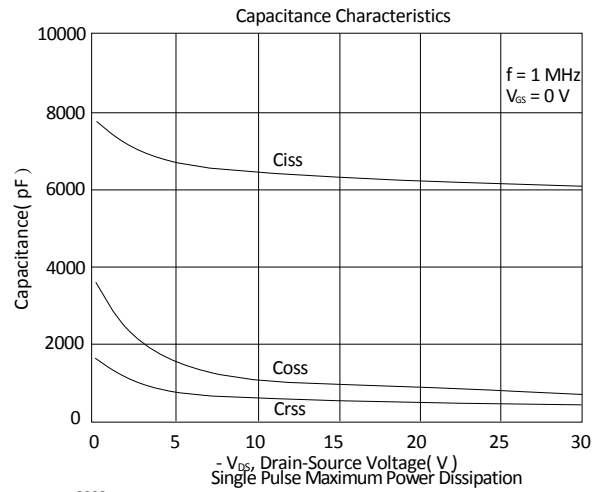
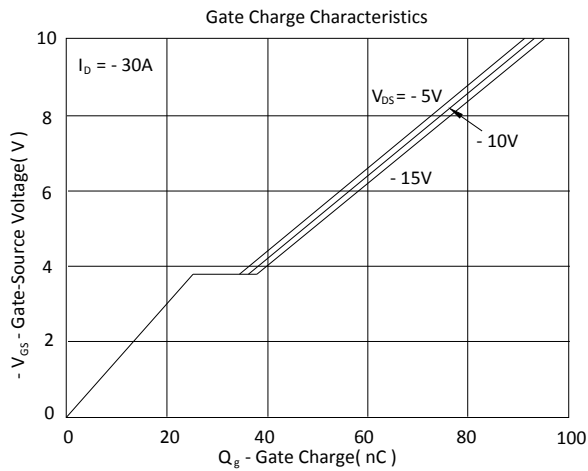
¹Pulse test : Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

²Independent of operating temperature.

³Pulse width limited by maximum junction temperature.

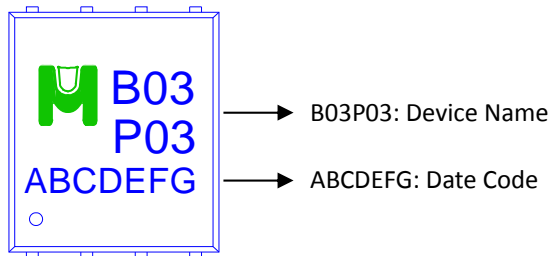
EMC will review datasheet by quarter, and update new version.



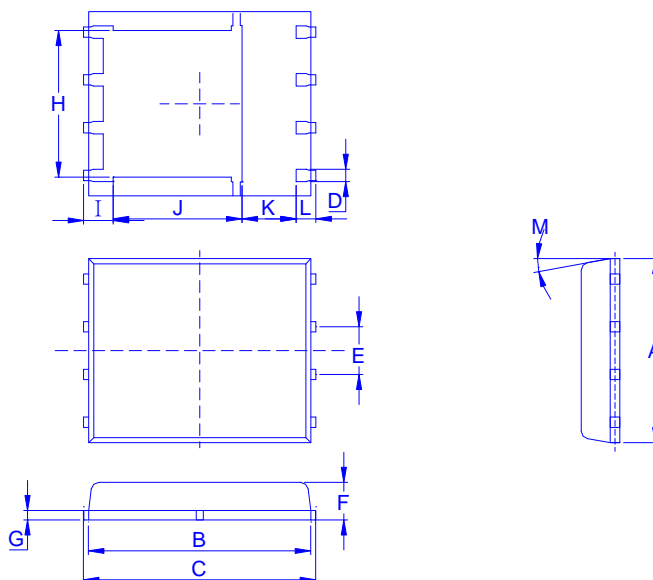


Ordering & Marking Information:

Device Name: EMB03P03H for EDFN5X6



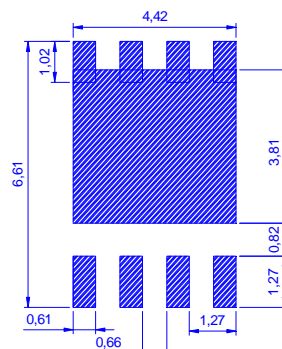
Outline Drawing



Dimension in mm

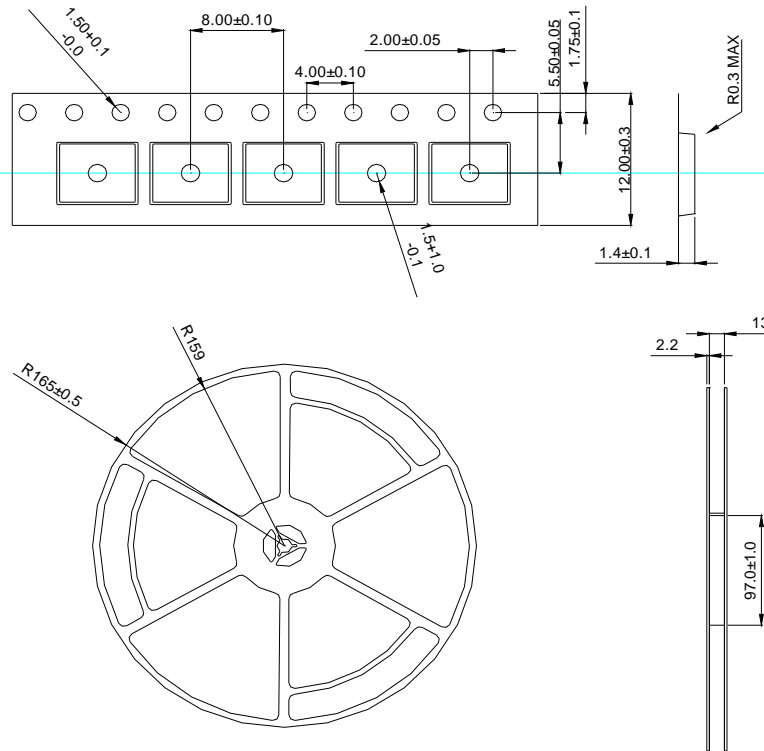
Dimension	A	B	C	D	E	F	G	H	I	J	K	L	M
Min	4.80	5.55	5.90	0.30	1.17	0.85	0.15	3.61	0.38	3.18	1.00	0.38	0°
Typ.	4.90	5.70	6.00	0.40	1.27	0.95	0.20	3.87	0.40	3.44	1.20	0.40	
Max	5.40	5.85	6.15	0.51	1.37	1.17	0.34	4.31	0.71	3.78	1.39	0.71	12°

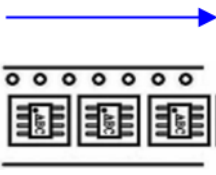
Recommended minimum pads





◆ Tape&Reel Information:2500pcs/Reel(Dimension in millimeter)



產品別	EDFN5X6
Reel 尺寸	13"
編帶方式	FEED DIRECTION 
前空格	25
後空格	50
裝箱數	
滿捲數量	2.5K
捲/內盒比	1 : 1
內盒滿箱數	2.5K
內/外箱比	10 : 1
外箱滿箱數	25K